Vivekanand College, Kolhapur
(An Empowered Autonomous Institute)
Department of Electronics
Internal Examination Notice

Date: 05/03/2026

All students of B.Sc. Part - I are hereby informed that their internal examination for Semester - II will be conducted in offline mode as per the schedule.

Paper Code	Section Title	Marks	Date	Time
2DSC03ELE21	Analog Electronics	10	13/03/2026	03:00 PM
2DSC03ELE22	Digital Electronics	10	13/03/2026	03:30 PM

(Prof. Dr. C. B. Patil)
HEAD
DEPARTMENT OF ELECTRONICS
VIVEKANAND COLLEGE, KOLHAPUR
(EMPOWERED AUTONOMOUS)

VIVEKANAND COLLEGE KOLHAPUR (Empowered Autonomous) ESTD JUNE 1964

Sem - II

Shri Swami Vivekanand Shikshan Sanstha's
VIVEKANAND COLLEGE, KOLHAPUR
(An Empowered Autonomous Institute)
Electronics Internal Exam Attendance
CLASS : B.Sc PART -I (NEP 2.0) SEM II 2025-2026
Date: 13/03/2026

Sr. No.	Roll No	Name of Students	2DSC03ELE21	2DSC03ELE222
1	7233	ANGANE DIVYA SHAMRAV	AB	AB
2	7234	BAGWAN HEENA HANJALA	Bagwan	Bagwan
3	7235	BODAKE SANIKA SATISH	Sanika	Sanika
4	7236	CHANDANSHIVE SIDDHARTH SANTOSH	Chandanshive	Chandanshive
5	7237	DARAGADE SRUSHTI SURESH	S.S.Daragade	S.S.Daragade
6	7238	GAIKWAD SHIVTEJ SACHIN	Gaikwad...	Gaikwad...
7	7240	GAVADE DIPAK BIKAJI	Gavade	Gavade
8	7241	GURAV ONKAR MAHESH	AB	AB
9	7244	JAHDAV PARTH PRAKASH	AB	AB
10	7245	JARALI ABHAY SHANKAR	Jarali...	Jarali...
11	7246	KAMBLE HARSHAD GANPATI	Kamble	Kamble
12	7247	KHARAPE ARJUN BAJARANG	AB	AB
13	7249	LAGARE AKASH ANANDA	AB	AB
14	7250	LOHAR SUSHANT SUBHASH	AB	AB
15	7251	MALI VIJAY HANAMANT	AB	AB
16	7252	MIRJE KAIVALYA ABHINANDAN	...	...
17	7253	MULANI TAHIRHUSSAIN RAJU	AB	AB
18	7254	PAGARE SARTHAK SANJAY	AB	AB
19	7255	PANDIT ADITYA MAHADEV	...	...

VIVEKANAND COLLEGE KOLHAPUR (Empowered Autonomous)

Sr. No.	Roll No	Name of Students	Date: 13/03/2026	
			2DSC03ELE21	2DSC03ELE222
20	7256	PATIL PRATHMESH SATISH		
21	7257	PATIL VIGHNESH NARAYAN		
22	7258	PATIL SAHIL DAGADU	AB	AB
23	7259	POWAR MANDAR PRATAP	AB	AB
24	7260	RAUT ANIKET SATISH	AB	AB
25	7261	SHAH NAMIT RAJENDRA		
26	7263	TEVARE ADITI SADASHIV	AB	AB
27	7264	PATIL ADITI SAHEBRAO		
28	7268	PATIL KSHITIJ RAVINDRA		
29	7283	ANGAJ OM LAHU	AB	AB
30	7284	BAVADEKAR ARYAN ANANDA		
31	7285	BHALEKAR JANHAVI SANDEEP		
32	7286	BIRANJE SUYASH UDAY		
33	7287	DEMANNA PIYUSH SURESH		
34	7288	GHADAGE ATHARV RAJESH		
35	7289	JADHAV PARAS RAMDAS		
36	7290	MANE SHREYASH YUVRAJ		
37	7291	MANE TUSHAR SANTOSH		
38	7292	MOMIN MAHAMMADANAS ASHPAK		
39	7293	PATIL ANIKET NAMDEV		
40	7294	PRABHU OM YASHWANT		
41	7296	AGALE SAMRUDDHI HINDURAV	S.H.Agale.	S.H.Agale.

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Sr. No.	Roll No	Name of Students	Date: 13/03/2026	
			2DSC03ELE21	2DSC03ELE222
42	7297	AWATE SARVASVI SWAPNIL	Sawate	Sawate
43	7298	BEDAGE SAMRUDDHI SANJAY	Bedge	Bedge
44	7299	DESHINGE VASUNDHARA MARUTI	Deshinge	Deshinge
45	7300	HAJGULKAR SALONI SURESH	AB	AB
46	7301	HEBBALI RITISHA SANTOSH	AB	AB
47	7302	JADHAV SANJANA ASHWIN	Jadhav	Jadhav
48	7303	KALANTRE PRANALI SARJERAO	Kalantre	Kalantre
49	7304	PATIL MANALI DEVAPPA	Patil	Patil
50	7305	PATIL SANSKRUTI DHIRAJ	Patil	Patil
51	7307	SATALE PRAGATI UTTAM	Satale	Satale
52	7308	TAMBOLI MARIYA RIYAJ		
53	7309	WADKAR NIKITA VISHWAS	Wadkar	Wadkar
54	7310	WARKARI SRUSHTI DAGADU	Warkari	Warkari
55	7311	BARGE ABHILASHA BAJIRAO	A.B. Barge	A.B. Barge
56	7313	BHINGARDE AARYA SANTOSH	A.S. Bhingarde	A.S. Bhingarde
57	7314	BHOSALE NAMRATA NANDKUMAR	Bhosale	Bhosale
58	7315	DAVARI SURAJ EKNATH	Dawari	Dawari
59	7316	GAVALI JANHAVI TANAJI	J.T. Gavali	J.T. Gavali
60	7317	JAMDAR JYOTIRAJ INDRAJIT	Jamdar	Jamdar
61	7318	KORANE SHRAVANI SAKHARAM	Shravani	Shravani
62	7319	MACHALE VIRAJ SANGRAM	Machale	Machale
63	7320	PATEL RUHI HARESH	Patel	Patel

VIVEKANAND COLLEGE KOLHAPUR (Empowered Autonomous) ESTD JUNE 1964

Sr. No.	Roll No	Name of Students	Date: 13/03/2026	
			2DSC03ELE21	2DSC03ELE222
64	7321	PATIL NAKSHATRA SAMADHAN	Patil	Patil
65	7322	PATIL PRASANNA HARISHCHANDRA	Patil	Patil
66	7323	PATIL SHREYASH MARUTI	S.M.P	S.M.P
67	7324	PATIL VEDIKA DEEPAK	Patil	Patil
68	7325	PEDNEKAR ASMITA BABURAO	Apednekar	Apednekar
69	7326	TAMHANEKAR ARPITA DHANAJI	Arpita.	Arpita
70	7327	TIKUDAVE SIDDHI NILESH	SNT	SNT
71	7497	PATIL AYUSH ASHOK	AB	AB
72	7562	PATIL KETKI AMIT	Ketki	Ketki
73	7566	JADHAV SHUBHAM RAJENDRA	AB	AB
74	7569	GUJAR VEDIKA DHANAJI	Vedika	Vedika
75	7571	PATIL KEDAR BABASO	AB	AB
76	7573	PATIL ATHARV DATTATRAYA	AB	AB
77	7579	KADAM PAWAN BAJIRAV	AB	AB
78	7583	NIGADE PARTH MANOHAR	AB	AB
79	7588	MUSHRIF ALFIYA KAMAAL		
80	7593	SAVANT PIYUSH PUNDALIK	AB	AB
81	7595	NIGADE HARSHVARDHAN RAVIRAJ	AB	AB
82	7606	MALAI SHREYA SHANKAR	Smalai	Smalai

VIVEKANAND COLLEGE KOLHAPUR (Empowered Autonomous)
ESTD JUNE 1964

Sem - II

VIVEKANAND COLLEGE, KOLHAPUR

(AN EMPOWERED AUTONOMOUS INSTITUTE)

Class: B.Sc.-I, Semester-II,

Subject and Course code: Analog Electronics- II 2DSC03ELE21

Time: **Date:-13/03/2025** **Marks: 10**

Q.1. Select the correct alternative **(2)**

i. A transistor is a ..... operated device

a) current b) voltage

c) both voltage and current d) none of the above

ii. The emitter of a transistor is ..... doped

a) lightly b) heavily

c) moderately d) none of the above

Q.2 .Attempt any Two (Four mark each) **(8)**

1) Explain Common Emitter configuration.

2) Define α and β? Derive the relation between them.

3) Explain construction and working of PNP transistor.

4) Explain construction and working of NPN transistor

VIVEKANAND COLLEGE, KOLHAPUR

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Class: B.Sc.-I, Semester-II,

Subject and Course code Digital Electronics- II 2DSC03ELE22

Time: Date:-13/03/2025 Marks: 10

Q.1.Select the correct alternative **(2)**

1. Positive edge-triggered flip-flop changes its state when _____ .

   a) Low-to-high transition of clock b) High-to-low transition of clock

   c) Enable input (EN) is set d) Preset input (PRE) is set

2. When the set is disabled (0) and reset is enabled (1) in S-R flip flop then the output will be _____

   a) set b) reset

   c) no change d) inderminate

Q.2.Attempt any two (Four marks each) **(8)**

1. Explain working of clocked RS flip-flop with logic diagram and truth table
2. Describe the working of JK flip flop with circuit diagram and truth table
3. Describe the working of D flip flop with circuit diagram and truth table
4. Explain the Master-Slave Flip-Flop with proper logic diagram. How it overcome the race condition of J-K flip-flop

Sem - II

Name :- Aditya Mahadev Pandit.

Student's Sign : Aditya

Seat No./ Roll No. : 7255

Seat No./ Roll No. In words : Seven two five five 06596

08/10

Digital Electronic.

प्र. क्र. Q. No.

Q.1

1] positive edge triggered flip-flop changes it's state when

→ (a) low-to-high transition of clock

2] when the set is disabled (0) and reset is enabled (1) in S-R flip-flop then the output will be

→ (b) Reset.

02

Marks 03

प्र. क्र.
Q. No.

2]

J-K flip-flop

:. constreuction

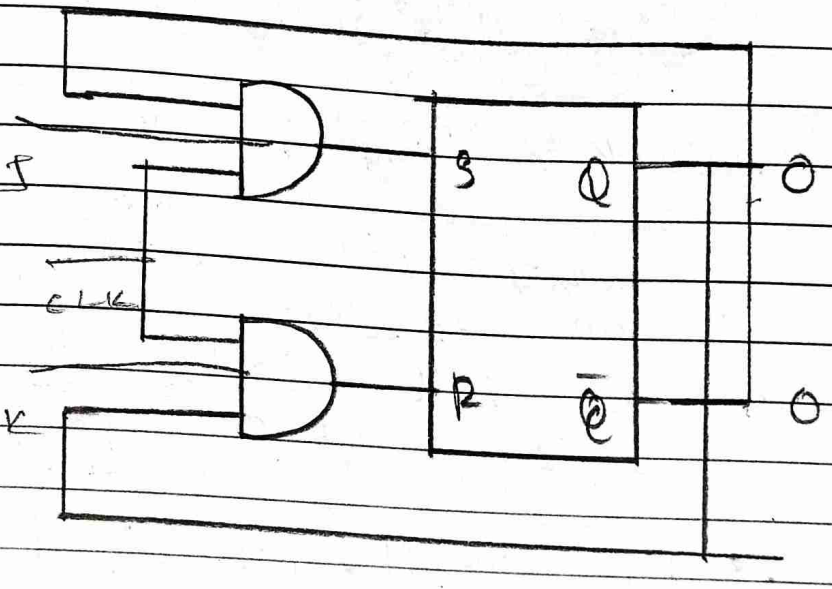
1. when J=0 & K=0 the output remains unchanged

2. when J=0 & K=1 the flip-flop reset (Q=0).

3 when J=1 & K=0 the flip seats (Q=1).

4. when J=1 & K=1 the output toggling 0 becomes & 1 become 0)

03



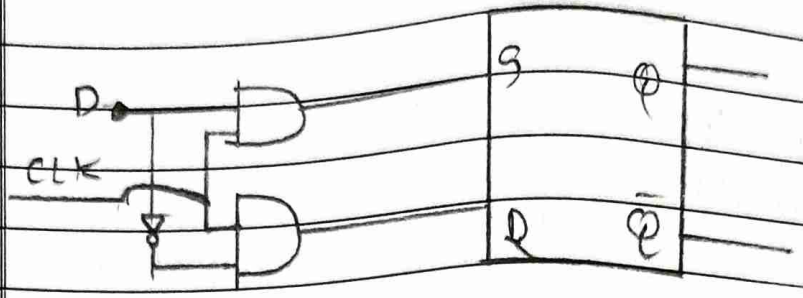
CLR	Input		Output
0	J	K	Qn+1
1	0	0	Qn
1	0	1	0
1	1	0	1
1	1	1	toggling

04 Section | Q. No. | Marks

— 2

प्र. क्र. Q. No.

87.



CLK	D	S	R	Q	$\bar{Q}$
0	X	0	0	Qn+1	
1	1	1	0	1	0
1	0	0	1	0	1

- the D flip flop is used to store high (1) bit or (0) low bit it is a solution to avoid for bidden state of flip-flop
  It's constructed by adding a not gat and
- only D as signal

- when clock = 0 both AND gate is disable.
  ∴ S=0 & R=0 i.e the flip-flop ~~gate and~~ goes to last state $Q_{n+1} = Q$.

- when clock = 1, these are two condition.

03

1] where D=1
the upper is ~~disable~~ enable AND
Lower and AND gate is disable.
∴ S = 1 and R = 0.

- i.e the flip-flop is set i.e Q = 1 $\bar{Q}$ = 0.

2] when D = 0.
the upper AND gate is disable. and
Lower.
∴ S = 0 & R = 1
i.e flip-flop is Reset i.e Q = 0, $\bar{Q}$ = 1.

॥ ज्ञान, विज्ञान आणि सुसंस्कार यांसाठी शिक्षण प्रसार ॥
- शिक्षणमहर्षी डॉ. बापूजी साळुंखे

कोल्हापूर १९६४

Digital Electronics
VIVEKANAND COLLEGE, KOLHAPUR
(An Empowered Autonomous Institute)
Assignment

10/10

Student's Sign :

Seat No./ Roll No. : 7252

Seat No./ Roll No. In words : Seven Two Five Two

06592

प्र. क्र. Q. No.

Q1

i. Positive edge-triggered flip-flop changes it's state when a) Low-to-High transition of clock

ii. When the set is disable (0) and reset is enable (1) in S-R flip-flop then the output will be (b) resket

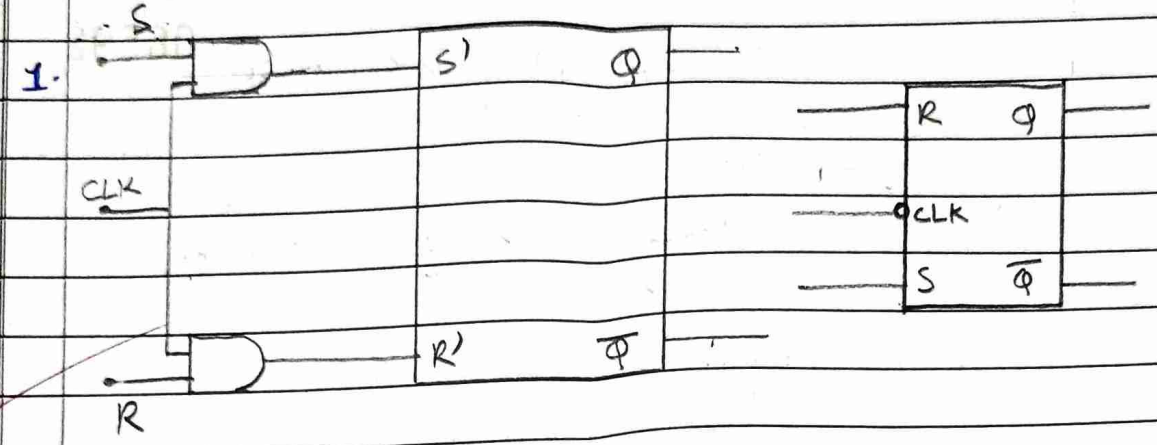
02

02 Section | Q. No. | Marks

प्र. क्र.
Q. No.

Q2

1.



- By The RS Flip-Flop uses two AND gates and CLOCK signal to Enable and disable SR signals.

- When Clock signal(CLK) is=0 both and gates are disable i.e output of both AND gate is 0 i.e S=R=0 this is last state which means Q = Last value

- When CLK=1 there are 4 states or conditions.

1) S=0 & R=0 ∴ S'=0 & R'=0
This state is Last state and will show last state on Q
$Q_{n+1} = Q$

2) S=0 & R=1
In this state The upper AND gate Enables
∴ S'=0 & R'=1

प्र. क्र.
Q. No.

Q2

1) 2) The Flip-Flop goes into Reset condition
$Q = 0$, $\overline{Q} = 1$

3) $S = 1$ & $R = 0$
i.e The Lower AND gate enables
∴ $S' = 1$ and $R = 0$
In This condition The Flip-Flop goes into Set condition $Q = 1$, $\overline{Q} = 0$

4) $S = 1$ & $R = 1$
i.e Both AND gate enable
∴ $S' = 1$ & $R' = 1$
This is known as Race condition or Forbidden in this state the output are random

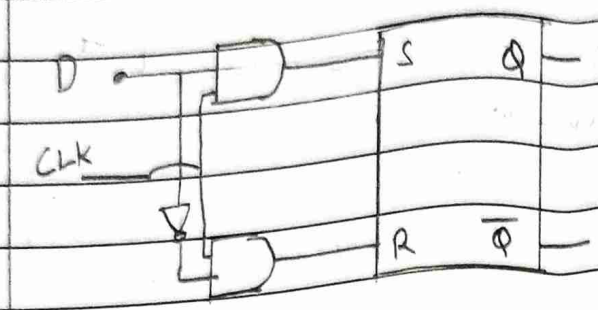
CLK	R	S	Q	$\overline{Q}$
0	x	x	L.S	L.S
1	0	0	$Q_{n+1} = Q$	L.S
1	0	1	1	0
1	1	0	0	1
1	1	1	Forbidden	

04 Section | Q. No. | Marks

प्र. क्र.
Q. No.

Q2

3.



CLK	D	S	R	Q	$\bar{Q}$
0	x	0	0	$Q_{n+1}=Q$	L.S
1	1	1	0	1	0
1	0	0	1	0	1

- The D Flip-Flop is used to store high (1) bit or (0) low bit, it is a solution to avoid forbidden state of Flip-Flop It is constructed by adding a not gate and only D as signal

When Clock = 0 both AND gate is disable
∴ S=0 & R=0 i.e the Flip-Flop goes into Last state $Q_{n+1} = Q$

- When clock = 1, There are Two conditions.
  1) When D=1
     The upper is enable AND Lower AND gate is disable
     ∴ S=1 and R=0
     i.e the Flip-Flop is set i.e Q=1, $\bar{Q}$=0
  2) When D=0
     The upper AND gate is disable and lower AND is enable
     ∴ S=0 & R=1
     i.e Flip-Flop is Reset i.e Q=0, $\bar{Q}$=1

Samruddhi Hinge

॥ ज्ञान, विज्ञान आणि सुसंस्कार यांसाठी शिक्षण प्रसार ॥
- शिक्षणमहर्षी डॉ. बापूजी साळुंखे

10/10

VIVEKANAND COLLEGE, KOLHAPUR
(An Empowered Autonomous Institute)
Assignment

Student's Sign : S.H.Agale
Seat No./ Roll No. : 7296
Seat No./ Roll No. In words : Seven thousands two hundred Ninety six
06510

प्र. क्र. Q. No.

Analog Electronics - II

Q.1

i) a) current

ii) b) heavily

Q.2

(2) Define α and β →

The ratio of collector ~~corre~~ current to the emitter current is called dc current gain. It is denoted by α_{dc}.

$$\therefore \alpha_{dc} = \frac{I_C}{I_E}$$

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The ratio of collector current to the base current is called dc current gain. It is denoted by β_{dc}.

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प्र. क्र.
Q. No.

$\therefore \beta_{dc} = \frac{I_c}{I_B}$

Relation between α_{dc} and β_{dc}

Since we know, $I_E = I_B + I_c$ ... (1)

$\alpha_{dc} = \frac{I_c}{I_E}$ ... (2)

$\beta_{dc} = \frac{I_c}{I_B}$ ... (3)

$\therefore I_E = I_B + I_c$

Dividing by I_c on both sides,

$\therefore \frac{I_E}{I_c} = \frac{I_B}{I_c} + 1$

$\therefore$ From eqn (2) & (3),

$\frac{1}{\alpha_{dc}} = \frac{1}{\beta_{dc}} + 1$

$\therefore \frac{1}{\alpha_{dc}} = \frac{1 + \beta_{dc}}{\beta_{dc}}$

$\therefore \boxed{\alpha_{dc} = \frac{\beta_{dc}}{1 + \beta_{dc}}}$

प्र. क्र.
Q. No.

Now, $\frac{1}{\alpha_{dc}} = \frac{1}{\beta_{dc}} + 1$

$\therefore \frac{1}{\alpha_{dc}} - 1 = \frac{1}{\beta_{dc}}$

$\therefore \frac{1}{\beta_{dc}} = \frac{1-\alpha_{dc}}{\alpha_{dc}}$

$\therefore \boxed{\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}}}$

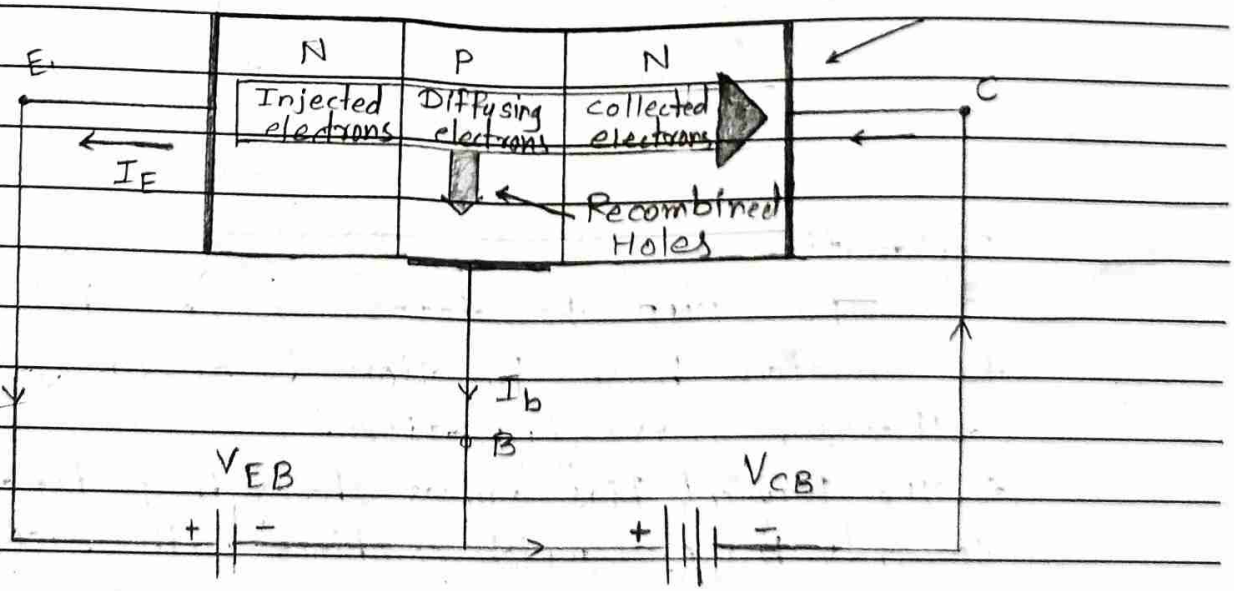
$\therefore$ Relation of α & β.

$$\alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}}$$

$$\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}}$$

4

④ Diagram →



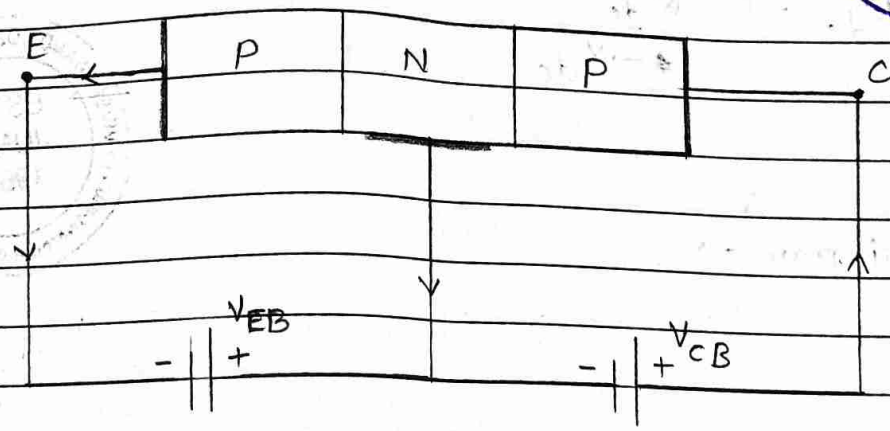
04 Section | Q. No. | Marks

प्र. क्र.
Q. No.

Explain →

① The NPN Transister with forward bias to emitter base junction and reverse bias to collector base junction.
② The forward bias causes the electrons in N-type emitter to emits electrons to the base.
③ The consists of I_E current.
④ The electrons combines with holes.
⑤ As the base is lightly doped and thin.
∴ The few electrons combines with holes (less than 2%)
⑥ It consists of I_B current.
⑦ Remainder electrons (more than 98%) cross to the collector.
⑧ It consists of I_C current.

⑤ Diagram →



Explanation →

① The PNP transister withe the forward bias to emitter base junction & reverse bias to collector base junction.
② The forward bias causes holes in p-type which flow towards base. which combines with electrons.