VIVEKANAND COLLEGE, KOLHAPUR

(An Empowered Autonomous Institute)

B.Sc. Part-I (Electronics) (Sem-II)

Internal Examination March-2025

Course name & Course Code: Digital Electronics-II: 2DSC03ELE22

Date: 11/03/2025 Time: 30 min

Marks: 10

Q.1) Select the correct alternative (one mark each) **(02)**

1. Positive edge-triggered flip-flop changes its state on _____ .
   a. Low-to-high transition of clock
   b. High-to-low transition of clock
   c. Enable input (EN) is set
   d. Preset input (PRE) is set
2. The Preset and Clear are _____-inputs in the flip-flops.
   a. Synchronous
   b. Asynchronous
   c. Control
   d. None of the Mentioned

Q.2) Attempt any TWO (4 marks each) **(08)**

1. Explain working of RS Latch using NOR gates
2. Explain working of D flip-flop with suitable diagram
3. Describe the working of JK flip flop with circuit diagram and truth table
4. What is the role of preset and clear terminal of flip-flop with suitable example?

Shri Swami Vivekanand Shikshan Sanstha's

VIVEKANAND COLLEGE, KOLHAPUR (An EMPOWERED AUTONOMOUS INSTITUTE)

B.Sc. I Sem II Internal Exam March 2025

Paper: Digital Electronics-II Code: 2DSC03ELE22 Date: 11/03/2025

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6	7232	PARALE ABHISHEK SAMBHAJI	
7	7233	PATIL PRATIKSHA PRAKASH	AB
8	7234	RAM ARCHANAKUMARI DAROGA	AB
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25	7270	KUWALEKAR KOUSTUBH BHASKAR	Kaustubh
26	7271	LOKHANDE APURVA DILIP	ALokhande
27	7272	MALAGE PRATIKRAJ JAYKUMAR	Pmalage.
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45	7290	KUMBHAR SIDDHI UDAY	
46	7291	KUPALE AKSHAY SHIVAJI	AB
47	7292	PATIL AISHWARYA BABASO	
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52	7529	SHINDE SHREEYASH FIRO	
53	7530	KADAM PAVAN BAJIRAO	AB
54	7539	BELEKAR SHUBHAM ANI	AB
55	7550	Dinesh Dattatray Mane	
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05/10 [signature]

Name – Sa...
BSc – I (Sem II)
Subject – Digital Elec.
Course Code – 2DSC03ELE22

|| ज्ञान, विज्ञान आणि सुसंस्कार यासाठी शिक्षण प्रसार ||
– शिक्षणमहर्षी डॉ. बापूजी साळुंखे

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प्र. क्र. Q. No.

Q1)

1) Positive edge-triggered flip-flop change its state on
→ a) Low-to-high transistion of clock.

2) The Preset and Clear are ___ inputs in the flip-flop
→ c) Control.

1

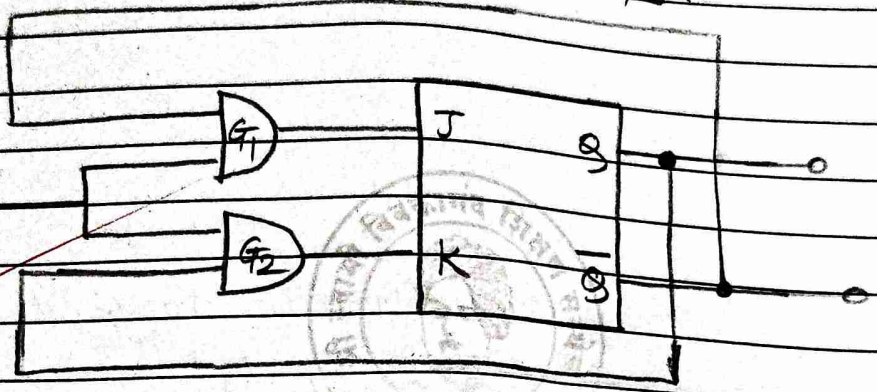
02	Section	Q. No.													
		Marks													

प्र. क्र.
Q. No.

Q2)

3)

⇒ Clocked JK flip flip [Level clocked].



A J-K Flip flop consists of two AND gates with inverted output signals compared to R-S Flip-flop. The Output conditions of AND gate is that if any of inputs is low then the output is also low.

Truth Table :

CLK	J	K	Action / Output
X	X	X	Qn (L.S)
0	X	X	Qn (L.S)
1	0	0	Qn (L.S)
1	0	1	0 (Reset
1	1	0	1 (set)
1	1	1	$\overline{Q}$n (L.S) / Toggle

प्र. क्र.
Q. No.

Working :

Case I : CLK = 0 (Low)

When CLK = 0, both J & K input signals enter do-not care condition, and their output signal reaches Last state

Here Q_{n+1} ⇒ Output signal ~~before~~ after clock is low

Q_n ⇒ Output signal before clock is low.

Case II : CLK = 1 (High)

When clock is high the further following cases of input and output are obtained, which are given as-

a) J = 0, K = 0 (CLK = 1)

With both the inputs low (J = K = 0) the two AND gates G_1 and G_2 remain disabled according ~~th~~ to the condition of AND.

∴ $Q = \overline{Q} = Q_n$

Hence the output remains in Last state.

b) J = 0, K = 1 (CLK = 1)

With inputs J = 0, K = 1, the AND gate G_2 only get activated and G_1 remains disabled

∴ $Q = 0$, $\overline{Q} = 1$

This condition is called RESET condition.

c) J = 1, K = 0 (CLK = 1)

With J = 1, G_1 gates get active and gives $Q = 1$ and as K = 0 we get $\overline{Q} = 0$

This condition is called SET condition.

d) J = 1, K = 1

Both inputs J & K high, hence, both the AND gates G_1 and G_2 activate simultaneously. This condition is called Toggle and therefore is NOT ALLOWED

Chandrekar

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- शिक्षणमहर्षी डॉ. बापूजी साळुंखे

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Course :- 2DSC08ELE22
Digital Electronics - II

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08/10

प्र. क्र. Q. No.

Q.1

1. Positive edge-triggered flip-flop changes its state on

→ b) High-to-low transition of clock

2. The present & Clear are ~~inputs~~ asynchronous inputs in the flip-flop.

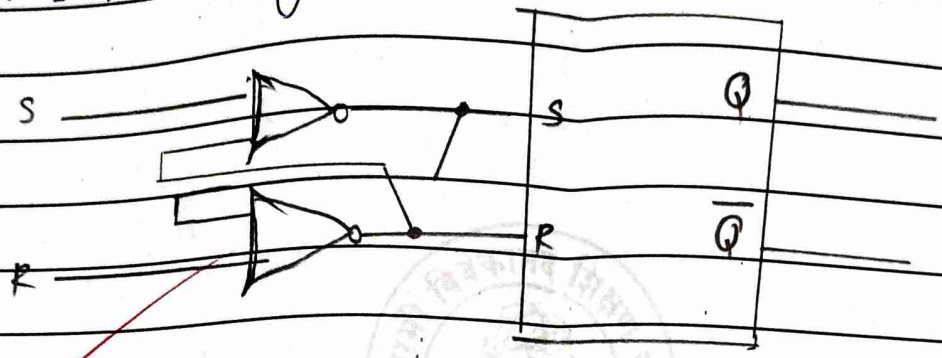
→ b) Asynchronous

02 Section | Q. No. | Marks

प्र. क्र.
Q. No.

Q. 2.

1. R-S Latch using NOR gates



Construction :-

- In R-S Latch two NOR gate are used
- ~~When the Input~~ In R-S Latch when one of input is high the output becomes low.

Working :-

Case - I :-

When R=0 & S=0

When R & S=0 they go on disabled & contain forbidden state or go in

Case II :-

When R=0 & S=1

When R=0 & S=1 then it is in set state

If ~~two~~ one output is high/1 the output 1 so it is in set state

When Case III :-

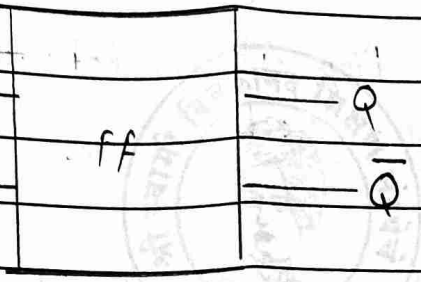
When R=1 & S=0

- When R=1 & S=0 then the output is is Reset state

Case IV :-

When R=0 & S=0

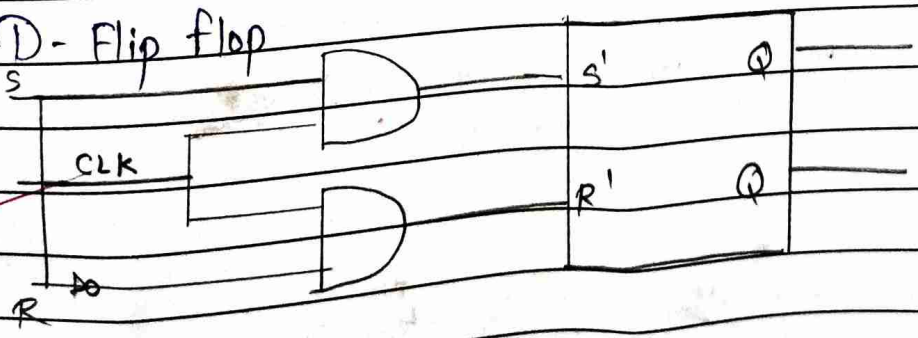
- When R=1 & S=1 then it is in L.S state it means Last state. It is completeary.



Logic of symbol

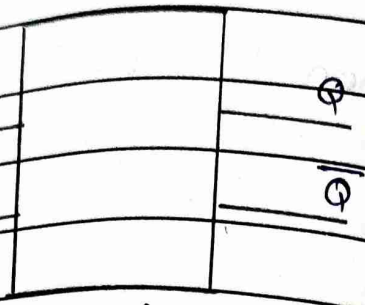
Input		Output	Action
R	S		
0	0	forbidden	Cross around
0	1	1	Set
1	0	0	Reset
1	1	L.S	No change

2) D- Flip flop



04 Section Q. No. Marks

प्र. क्र. Q. No.



Logic of symbol.

~~Working~~ :-

Consitruction :-

- In D. flip-flop it contist two AND & one NOR gate & also using clock ~~one input is~~ :

Working :-

Case I :-

When ~~D=0~~ CLK=0

- When CLK=0 it is not allowed it is ~~an~~ complentary 'Clear Pare'
- So it is in Last state.

Case II :-

When CLK = 1

It is an also Last state

So these are two state

1) D=0 :-

When ~~it is an~~ D=0 then it is an Set state.

2) D=1 :-

When D=1 then it is an Reset state

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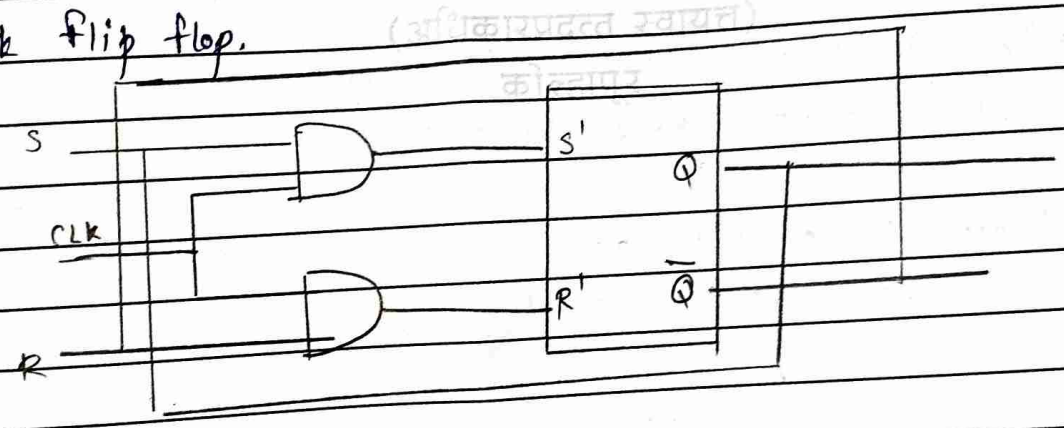
Input		Output
CLK	D	(Q_{n+1})
0	x	L.S (Q_n)
1	x	L.S (Q_n)
1	0	Set
1	1	Reset

3) Jk flip flop.



S		Q
CLK		$\overline{Q}$
R		

02 Section | Q. No. | Marks

प्र. क्र. Q. No.

Working :-

Case I :-

When CLK = 0

- When CLK is 0 is complementary state it is not allow so it is Last state

Case II :-

When CLK = 1

- When CLK is 1 it is not allowed it is also Last state

When CLK = 1 it has 4 Values

a) When R = 0 & S = 0

When R & S = 0 is also not allowed it is in L.S (Last state)

03

b) When R = 0 & S = 1

When R = 0 & S = 1 it is in Set state

c) When R = 1 & S = 0

it is Reset state

Shree Swami Vivekanand Shikshan Sanstha's

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Class: B.Sc.-I, Semester-II,

Course code: 2DSCO3ELE21 **Subject**: Analog Electronics II

Time: 02:00 pm to 02:30 pm **Date**:-10/03/2025 **Marks**: 10

Q.1.Select the Correct alternative **[2 M]**

i. The number of depletion layers in a transistor is .....

1. Four
2. Three
3. Two
4. One

ii. The region that has the biggest size in a transistor is .....

1. collector
2. base
3. emitter
4. collector-base-junction

Q.2 .Attempt any Two (Four mark each) **[8 M]**

1) Explain DC load line and Q-point.

2) Explain construction and working of NPN transistor.

3) Explain construction and working of PNP transistor.

4) Define α and β? Derive the relation between them.

Shri Swami Vivekanand Shikshan Sanstha's

VIVEKANAND COLLEGE, KOLHAPUR (An EMPOWERED AUTONOMOUS INSTITUTE)

B.Sc. I Sem II Internal Exam March 2025

Paper: Analog Electronics-II Code: 2DSC03ELE21 Date: 10/03/2025

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53	7530	KADAM PAVAN BAJIRAO	
54	7539	BELEKAR SHUBHAM ANI	
55	7550	Dinesh Pattatray Mane	
~~56~~	~~7241~~	~~Samruddhi Kaushal Pawar~~	~~Absent~~
	7548	AYYAN PATEL	
	7548	AYYAN PARVEJ PATEL	

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Date : 10/03/2025
Paper : Analog Electronics

VIVEKANAND COLLEGE, KOLHAPUR.

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Course code : 20SCOSELE21

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10/10

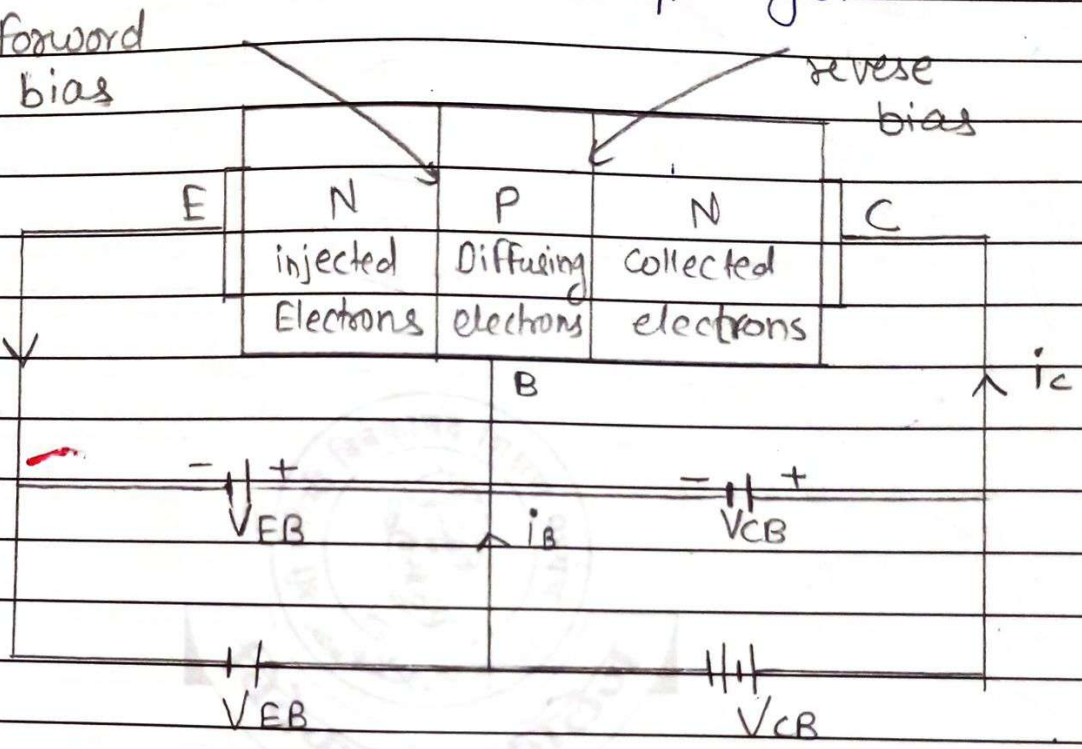
प्र. क्र. Q. No.		
1]	1]	3. Two
	2]	2. Collector

02 Section | Q. No. | Marks

प्र. क्र. Q. No.

2] ① NPN is a type of transistor where P-region of transistor is sandwiched between two N-type regions.

2]



② As shown in the figure forword bias to emitter base junction start flow of electrons towards P region. that causes to constitute current i_E. In P region Base is lightly doped because of that in P region just 2% of all flow of electrons entering from a become able to collaborat / intersect with holes in P. Remaining 98% electrons flow towards collector region. Diffusing process in P region constitute to i_B current flow. In collector region electrons that remaining in P are collected. because of this process they causes to constitute current i_C. The whole current I_E is divided in I_C and I_B. After observing that process we concluded that the Emitter current I_E is the sum of I_C and I_B.

Section | Q. No. | Marks

$$I_E = I_C + I_B \quad \text{— (I)}$$

Q. 2 4] (1) α is defined as the current gain of transistor to CB (common Base configuaration).

$$\alpha_{dc} = \frac{I_C}{I_E}$$

(2) β is defined as the current gain of transistor to CE (common Eimitter configuaration)

$$\beta_{dc} = \frac{I_C}{I_B}$$

(3) Relation between α and β.

we know the eqn

$$I_E = I_C + I_B \quad \text{— (I)}$$

let divide eqn (I) by I_C.

$$\frac{I_E}{I_C} = \frac{I_C}{I_C} + \frac{I_B}{I_C}$$

$$\frac{1}{\alpha_{dc}} = 1 + \frac{1}{\beta_{dc}}$$

$$\frac{1}{\alpha_{dc}} = \frac{\beta_{dc} + 1}{\beta_{dc}}$$

$$\boxed{\alpha_{dc} = \frac{\beta_{dc}}{1 + \beta_{dc}}} \quad \text{— (I)}$$

similaraly,

$$\frac{1}{\beta_{dc}} = \frac{1}{\alpha_{dc}} - 1$$

04 Section | Q. No. | Marks

प्र. क्र. Q. No.

$$\frac{1}{\beta_{dc}} = \frac{\alpha_{dc} - 1}{\alpha_{dc}}$$

$$\beta_{dc} = \frac{\alpha_{dc}}{(\alpha_{dc} - 1)} \quad \text{—(2)}$$

These both are the relation between α and β.

Class – BSc (I, Sem II)

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Subject – Analog Elec.
Code – 2DSC03ELE21

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प्र. क्र. Q. No.

Q1)

1) The number of depletion layers in a transistor is
→ ~~b) Three~~ c) Two.

C 1

2) The region that has the ~~highest~~ biggest size in a transistor is

→ 0

02 Section | Q. No. | Marks

प्र. क्र.
Q. No.

(Q2)
4)

⇒ a) α – The current gain between the common-emitter configuration is α. It is also defined as the ratio of collector current to the emitter current i.e I_C & I_E respectively.

$$\alpha = \frac{I_C}{I_E}$$

b) β – The current gain between the common-base configuration is called as β. It is also defined as the ratio of collector current to the base current i.e I_C & I_B respectively $\Rightarrow$

$$\beta = \frac{I_C}{I_B}$$

c) Relation between α and β

As we know that, $I_E = I_C + I_B$ ——— (I)

Emitter current is the sum of collector (cut-off) current and base current.

From the equation of α we get,

$I_C = \alpha \cdot I_E$ ——— (II)

And from the equation of β we get,

$I_B = \beta \cdot I_E$ ——— (III)

∴ Substituting eqn (II) & (III) in eqn (I) we get,

$I_E = \alpha I_E + \beta I_E$

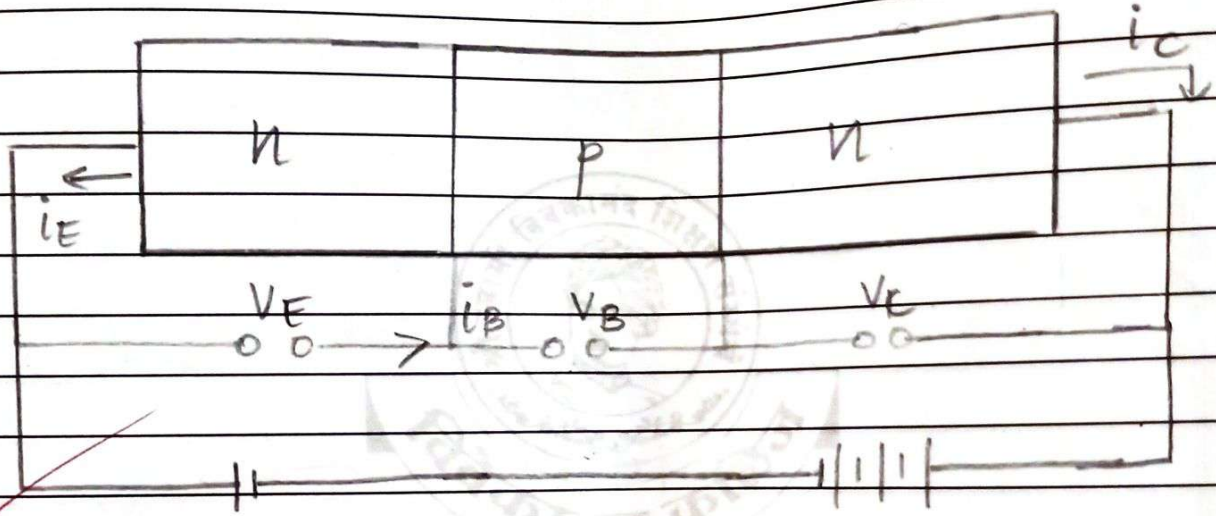
$I_E = (\alpha + \beta) I_E$

Section Q. No. Marks

$\therefore \quad \boxed{\alpha = 1 - \beta}$

or $\boxed{\beta = 1 - \alpha}$

Q2)



The above figure shows NPN transistor with emitter-base forward biasing and collector base reverse biasing. The electrons travel from n-region to p-region to combine with holes and gives rise to emitter current I_E in the direction shown in the figure. As the transistor is lightly doped and very thin, only 2% of electrons remain in p-region to combine with holes and the other remaining 98% travel to n-region to form collector current I_C.

This behaviour further tells that the emitter current is the summation of collector current & base current

$\therefore \quad \boxed{I_E = I_C + I_B}$