Vivekanand College, Kolhapur (Empowered Autonomous) Department of Electronics Notice

Date: 13.03.2024

All the students of B.Sc. II Electronics are hereby informed that their internal examination for Semester IV will be conducted in offline mode as per given schedule.

Paper Code	Section title	Marks	Date	Time
DSC1005D	Operational Amplifier	15	21-03-2024	03:50 pm-04.40 pm
	Microcontroller 8051	15	22-03-2024	02:10 pm-03.00 pm

(Dr. C. B. Patil)

HEAD
DEPARTMENT OF ELECTRONICS
VIVEKANAND COLLEGE, KOLHAPUR
SEMPOWERED AUTONOMOUS)

Vivekanand College, Kolhapur (Empowered Autonomous)

B.Sc. Part- II (Electronics) (Sem-IV) Internal Examination March 2023-24 Course Code: DSE - 1005D

Section - I: Operational Amplifier

Date: 21/03/2023	57	2	marks: 15
Q.1) Select most correct alternatives for	the following	(one mark each)	[3 Marks]
1. The input stage of an Op-amp is us	ually a		
A) differential amplifier	B)	CE amplifier	
C) CB amplifier	D)	CC amplifier	
2. An ideal op-amp hasoutpu	it impedance		
Α) 75 Ω		Ω	
C) 2M Ω	D) I	nfinite Ω	
An integrator op-amp uses A) resistor	element in the B)	capacitor	
C) inductor	D)	None of the above	
Q.2) Attempt any Three (Four marks each	ch)		[12 Marks]
1. Explain the open loop and close loo	p configuration	on of op-amp.	
2. Explain the common mode rejection	ratio (CMRF	R) and slew rate of op-	amp.
Explain the working of Op-Amp as			
4. Draw the circuit diagram of Op-Am	ip as a subtrac	tor and write the equa	non for output
voltage.			
5. Draw circuit diagram of op-amp in	inverting amp	lifier. Find the express	sion for its
output voltage & gain			
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Shri Swami Vivekanand Shikshan Sanstha's Vivekanand College, Kolhapur (Empowered Autonomous)

Class: B.Sc.-II, Semester-IV,

Internal Examination (2023-24)

DSC-1005D: Microcontroller 8051

Date:-22/03/2024 Marks: 15	Time: 02:10pm to 03:00pm
tests despring or	
Q. 1 Select correct alternative for the following:	$[3 \times 1 = 3]$
1. 8051 hasnumber of I/O 8 bit ports. A) 8 B) 32 C) 4 2. The range of short jump instruction is	D) 1
A) 0 to 255 B) -128 to 127 C) 0 to 2K 3instruction has Register addressing mode A) MOV A, R7 B) MOV A, @R1 C) ADD A,	e.
Q. Solve any ONE out of TWO:	$[1 \times 8 = 8]$
1. Explain the RAM and ROM structure/organization	of 8051.
Classify the instruction set according to function suitable examples.	ns and explain each with two
Q. Solve any ONE out of TWO:	$[1 \times 4 = 4]$
1. Explain the PSW register of 8051.	
2. Explain the DPTR register of 8051.	