LECTURE NOTES (E- CONTENTS) for

B.Sc. II Electronics (2021-22)

Semester: III Paper- III

DSC -1005 C Electronics Communication and Microprocessor 8085

Section II: Microprocessor 8085

Unit- 2: Architecture of 8085 Microprocessor

Prepared and Circulated for

B .Sc. II Electronics Students

BY

Dr. C. B. Patil

Assistant Professor, Department of Electronics

Vivekanand College (Autonomous), Kolhapur

UNIT 2
Architecture of 8085 Microprocessor

Syllabus: Architecture of 8085 Microprocessor: Silent features of 8085.Block diagram and Pin description of 8085. Data and address bus, Registers, ALU, Stack pointer, Program counter, Flag register, Clock and reset circuits. Interrupts in 8085. De-multiplexing of AD0-AD7. T-states, Machine cycle, Instruction cycle. Timing diagram of MOV and MVI instructions.

Introduction:

Microprocessor (μp) is a multipurpose, programmable logical device that reads binary instructions from memory, accepts binary data as an input & processes the data according to those instructions & provides the result as an output. Microprocessor is a semiconductor device consisting of several digital circuits, which performs together to execute the instructions given by the user. Depending upon the capability of handling a data, they are classified as 4-bit, 8-bit, 16-bit, 32-bit microprocessor. It can be used in two different ways.

1. as a programmable logic device to control the process.

   e.g. -VCRs, washing-machine, video game, T.V., microwave oven, copying machine, toys etc.

2. as a data processing unit or a computing units of a computer like P.C.

2.1 <u>Features of 8085:</u>

i. 8085μp was manufactured by INTEL.
ii. It is 40 pin IC manufactured using N-MOS technology.
iii. It is an 8-bit microprocessor i.e. it can accept, process or provide 8-bit data simultaneously.
iv. It operates on a single +5V power supply connected at Vcc
v. It has on chip clock generator. This internal clock generator requires tuned circuit like LC, RC or crystal. The internal clock generator divides oscillation frequency by 2 and generates clock signal, which can be used for synchronizing external devices.
vi. It can operate with 3 MHz clock frequency.
vii. It has 16 address buses; hence it can access 64 Kbytes (2^{16}) bytes of memory.
viii. In 8085, the lower 8-bit address bus (A0-A7) and data bus (D0-D7) are multiplexed to reduce number of external pins. But due to this, external hardware is required to separate address lines and data lines.
ix. It supports 74 instructions with following addressing modes. (a) Immediate, (b) Register, (c) Direct (d) Indirect (e) Implied.
x. The Arithmetic logic unit of 8085 performs a) 8 bit binary addition with or without carry. (b) 16 bit binary addition (c) 2 digit BCD addition (d) 8-bit binary subtraction with or without borrow (e) 8-bit logical AND, OR, EX-OR, complement (NOT) and bit shift operations.
xi. It has 8-bit accumulator, flag register, instruction, register, six 8-bit general purpose Registers (B, C, D, E, H and C) and two 16-bit registers (SP and PC)
xii. It provides control and status signals (RD, WR, IO /M ,S0, S1) to initiate different Machine cycle operations.
xiii. It provides five hardware interrupts: TRAP, RST 7.5. RST 6.5, RST 5.5 and INTR. It also has a mechanism by which it is possible to increase its interrupt handling capacity.
xiv. It has serial I/O control unit which allows serial communication.
xv. The external hardware (another microprocessor or equivalent master) can detect which machine cycle microprocessor is executing using status signals (IO/M, S0, S1). This feature is useful when more than one processors are using common system resources (memory & I/O devices).
xvi. The 8085 has an ability to share system bus with Direct Memory Access (DMA) controller. This feature allows transferring large amount of data from I/O device to memory or from memory to I/O device with high speeds.

2.2 Internal Architecture of 8085 microprocessor:

Fig.2.1 shows internal architecture of 8085 µp. It includes accumulator, ALU, Control unit, instruction register, instruction Decoder & Encoder, Timing & control unit, Serial I/O control, Interrupt control unit etc.

Control Unit

Generates signals within µp to carry out the instruction, which has been decoded. In reality causes certain connections between blocks of the µp to be opened or closed, so that data goes where it is required, and so that ALU operations occur.

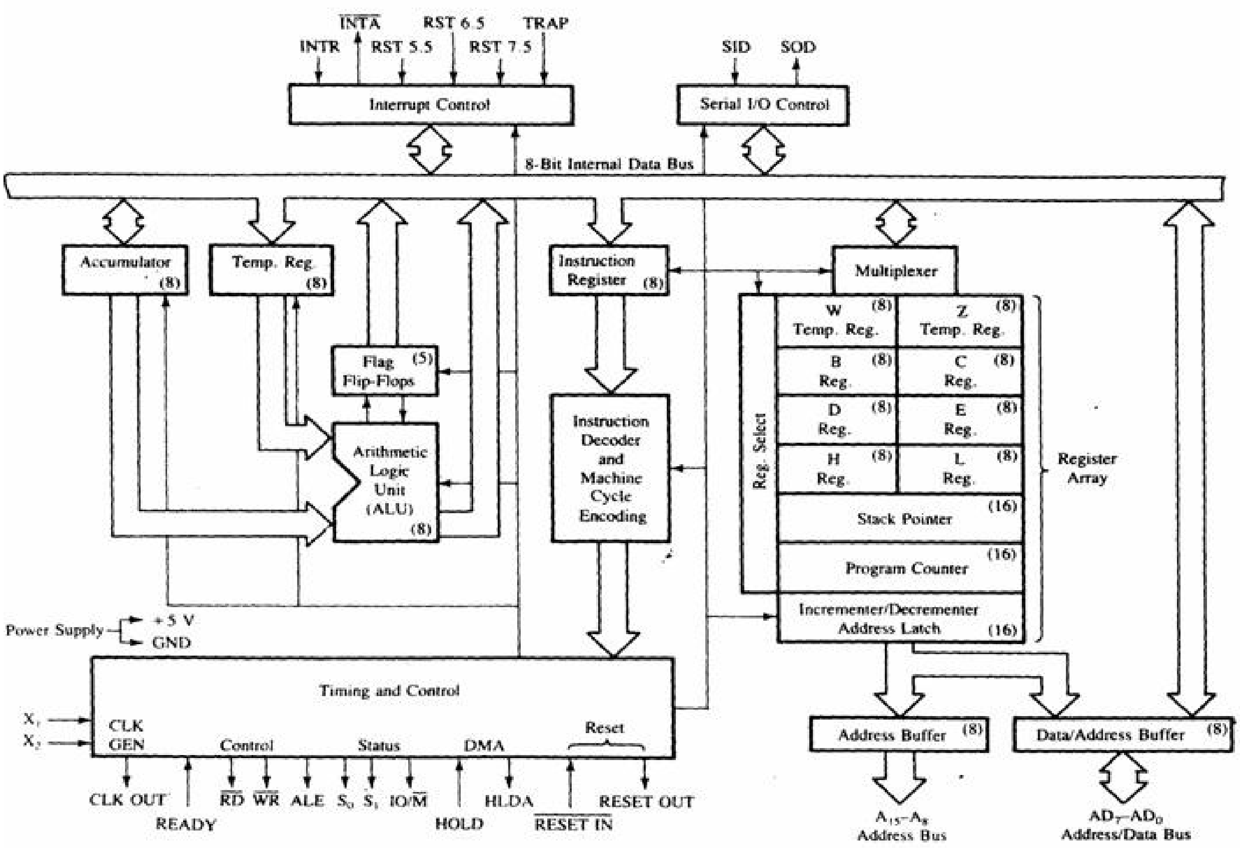


Fig. 2.1 Internal Architecture of 8085 microprocessor

Arithmetic Logic Unit

The ALU performs the actual numerical and logic operation such as 'add', 'subtract', 'increment', 'decrement', 'AND', 'OR', 'EX-OR' etc. It uses data from memory and from Accumulator to perform arithmetic and always stores result of operation in Accumulator.

Accumulator

It is one of the principal register. It is an 8-bit register identified as register A and it is a part of arithmetic/logic unit (ALU). It's functions are –

- It is one of the principal register.
- It is an 8-bit register identified as register A
- Most of the arithmetic and logic operations are performed using this accumulator.
- One of the operands for arithmetic operations in ALU is from the accumulator.
- After performing the arithmetic operations, the result is stored back in accumulator.
- All the I/O data transfers between 8085 and I/O devices are performed via accumulator.
- The data is sent out to an output device from the accumulator only.
- Similarly, the data from an input device is read only through the accumulator.
- The data in the accumulator alone can be rotated or shifted. No other register can be used for these operations.
- Certain instructions like DAA are performed using only accumulator.
- So, many times the Accumulator register is treated as a default register.

Temporary register:

- This is an 8-bit register which is not accessible to the user.
- This register is used by the microprocessor to load the second operand during arithmetic/logical operations in ALU.

- For example in ADD C instruction C register contents are moved to the Temp. Register and the addition of A and Temp. Register contents is performed by the ALU.
- For example when MVI M, 17H instruction is fetched, IR register will receive the opcode for MVI M and the Temporary register will receive 17H.

Flags

The ALU includes five flip-flops, which are set or reset after an operation according to data conditions of the result in the accumulator and other registers. They are called Zero (Z), Carry (CY), Sign (S), Parity (P), and Auxiliary Carry (AC) flags. The most commonly used flags are Zero, Carry, and Sign. The microprocessor uses these flags to test data conditions.

For example, after an addition of two numbers, if the sum in the accumulator is larger than eight bits, the flip-flop uses to indicate a carry called the Carry flag (CY) is set to one. When an arithmetic operation results in zero, the flip-flop called the Zero (Z) flag is set to one.

The figure 2.2 shows an 8-bit register, called the flag register. However, it is not used as a register; five bit positions out of eight are used to store the outputs of the five flip- flops. The flags are stored in the 8-bit register so that the programmer can examine these flags (data conditions) by accessing the register through an instruction. These flags have critical importance in the decision- making process of the microprocessor. The conditions (set or reset) of the flags are tested through the software instructions.

For example, the instruction JC (Jump on Carry) is implemented to change the sequence of a program when CY flag is set. The detail understanding of flag is essential in writing assembly language programs.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S	**Z**		**AC**		**P**		**CY**

Figure 2.2 Flag register

1. **Sign Flag (S):** After execution of any arithmetic and logical operation, if D7 of the result is 1, the sign flag is set [S =1]. Otherwise it is reset[S =0]. D7 is reserved for indicating the sign; the remaining is the magnitude of number. If D7 is 1, the number will be viewed as negative number. If D7 is 0, the number will be viewed as positive number.
2. **Zero Flag (z):** If the result of arithmetic and logical operation is zero, then zero flag is set [Z =1] otherwise it is reset [Z = 0].
3. **Auxiliary Carry Flag (AC):** If D3 generates any carry when doing any arithmetic and logical operation, this flag is set [AC =1] otherwise it is reset [AC =0] .
4. **Parity Flag (P):** If the result of arithmetic and logical operation contains even number of 1's then this flag will be set [P =1] and if it is odd number of 1's it will be reset[P =0] .
5. **Carry Flag (CY):** If any arithmetic and logical operation result any carry then carry flag is set [CY =1] otherwise it is reset[CY =0] .

Temporary registers:

- W and Z are also temporary registers used to hold 8-bit data during execution of certain instructions.
- As these registers are internally used by the CPU, they are not accessible to the user.
- The W and Z registers are used by the processor during CALL instruction. When a CALL instruction is encountered in any program, the current Program counter (PC) contents are pushed on to the stack and the given address is loaded on to PC.The given address is temporarily stored in W and Z registers and placed on the bus for the fetch cycle. Thus the program control is transferred to the address given in the instruction.
- Another example is, during the execution of XCHG instruction, the contents of H-L pair are exchanged with D-E pair. At the time of exchange W and Z registers are used for temporary storage of data.

General Purpose Registers

The 8085 has six general-purpose registers to store 8-bit data; these are identified as B, C, D, E, H and L. They can be combined as register pairs - BC, DE, and HL to perform some 16-bit operations. The programmer can use these registers to store or copy the data into the registers by using data copy instructions. The 8085 programming model also includes one accumulator, and one flag register. In addition, it has two 16-bit registers: the stack pointer and the program counter.

Program Counter (PC)

This 16-bit register deals with sequencing the execution of instructions. This register is a memory pointer. Memory locations have 16-bit addresses, and that is why this is a 16-bit register. The microprocessor uses this register to sequence the execution of the instructions. The function of the program counter is to point to the memory address from which the next byte is to be fetched. When a byte (machine code) is being fetched, the program counter is incremented by one to point to the next memory location.

- It is a 16-bit special purpose register
- This register is a memory pointer used to sequence the execution of the instructions from memory device.
- The execution of a program is initiated by loading the PC by the address of the first instruction of the program.
- Once the byte is fetched, the PC is automatically incremented to point to the next byte unless a jump to some specific address occurs.
- This process is repeated till the last instruction of the program.
- In case of JUMP or CALL instructions, current address is stored on to the Stack and new address specified by the JUMP or CALL instruction is loaded in the Program Counter. So now execution goes to new address specified by the JUMP or CALL instruction.

Stack Pointer (SP)

The stack pointer is also a 16-bit register used as a memory pointer. It points to a memory location in R/W memory, called the stack. The beginning of the stack is defined by loading 16-bit address in the stack pointer. It always points to top of the Stack

Instruction Register, Decoder & Encoder

The current instruction from memory is stored in Instruction Register (IR) before execution. Decoder then takes instruction and 'decodes' or interprets the instruction. Decoded instruction then passed to next stage. Encoder generates the sequential control signals.

Timing & control unit

This unit synchronizes all the µp operations with the CLK & generates the different control signals for communication between µp & peripherals.

Interrupt control unit

An interrupt can be defined as any signal to the µP that alters the normal sequence of execution of a program. The interrupt can be introduced in the µP through an instruction written in the program or it can even be initiated by external device. Whenever µP receives any interrupt it's control gets shifted to some other location in order to execute a set of instructions called service routine which is written at that location. The µP resumes its operation after completing the service routine. The interrupt process in 8085 is controlled by the Interrupt Enable flip-flop, which is internal to the processor and can be set or reset by using software instructions. There exist two types of interrupts: a) Software interrupts b) Hardware interrupts

i. **Software interrupts**

The instruction set of 8085 includes eight RST (Restart) instructions referred to as software interrupts. These are one-byte instructions. Each of these instructions allows the transfer of the program execution to a specific location on page 00H. Therefore RST instructions act like a vector that points towards different memory locations.Table1 shows the list of different RST instructions.

The RST0 instruction service routine is stored in locations between 0000H and 0007H. When this instruction is given the Program Counter (PC) points to the memory location 0000H and its current address is loaded into the stack pointer. After the service routine is executed the PC returns back to the address of the next memory location by popping back the address from the stack pointer. Similarly RST1 service routine is stored in memory location 0008H to 000FH. In the same way when RST5 is inserted in the program it transfers the control to memory location 0028H. It is a break point service routine. The RST5 instruction displays the contents of accumulator and the flags when the A key is pressed and returns to the calling program when the

Zero key is pressed.

Instruction	Hex Code	Vector location
RST0	C7	0000H
RST1	CF	0008H
RST2	D7	0010H
RST3	DF	0018H
RST4	E7	0020H
RST5	EF	0028H
RST6	F7	0030H
RST7	FF	0038H

Table 2.1: Software Interrupts and their vector locations

ii. **Hardware interrupts**:

The 8085 microprocessor has five interrupts. They are TRAP, RST 7.5, RST 6.5, RST5.5 and INTR. The following section gives the detail description of all the 8085 interrupts.

Interrupt Name	Trigger Type	Priority	ISR Address	Vectored	Maskable
TRAP	Edge and level	Highest (1)	0024H	YES	NO
RST 7.5	Edge	2^{nd}	003CH	YES	YES
RST 6.5	Level	3^{rd}	0034H	YES	YES
RST 5.5	Level	4^{th}	002CH	YES	YES
INTR	Level	Least (5^{th})	Not specific	NO	YES

Table 2.2: hardware Interrupts and their vector locations

The interrupts are also classified as:

a) **Vectored interrupts:** Vectored interrupts are the ones which have some specific memory locations on page 00H associated with them and the control is automatically transferred to the respective memory location without any external hardware. Example of vectored interrupt is RST5.5, RST6.5, RST7.5 and TRAP.

b) **Non-vectored interrupts:** Non-vectored interrupts are the ones in which user has to specify the address along with the interrupt where the control is to be transferred. Example of non-vectored interrupt is INTR.

c) **Maskable interrupts:** Maskable interrupts are the one which µP need not attend immediately as and when it comes instead µP can ask it to wait for some time. Example of maskable interrupt is RST5.5, RST6.5, RST7.5 and INTR.

d) **Non-Maskable interrupts:** It is also known as NMI. It is the interrupt which µP has to attend as and when it comes i.e. it can’t be ignored or asked to wait. Example of non-maskable interrupt is TRAP.

<u>Serial I/O control</u>

- By using this unit the µp can communicate with serial devices.
- This control provides two lines SOD (Serial Out Data) and SID (serial In Data) for serial communication.
- These lines are used during serial data transmission over long distance where data is transmitted and received bit by bit.
- The Serial Output Data (SOD) pin is used to send data out serially and serial Input Data (SID) pin is used to receive data serially by the 8085 microprocessor.

2.3 8085 signal diagram

The 8085µp is 8 bit general purpose µp capable of addressing 64KB of memory. The device has 40 pins as shown in fig. 2.3 and requires +5V power supply & can operate with 3MHz clock frequency. The all signals are classified into different groups as shown in fig.2.4.

Address bus: The 8085µp has 8 signal lines A_8-A_{15} which are unidirectional & used to carry high order address.

Multiplexed Address/Data Bus:

The signal lines AD_0-AD_7 are bidirectional & serves two purposes i.e. these lines are used to carry low order addresses in earlier part of every operation & to carry data during later part of every operation.

Control signals:

1) RD (READ): This is active low output signal, used to read data from memor y or in I/O device.
2) WR (WRITE): This is active low output signal. It indicates the data on the Data Bus is to be written into the selected memory or I/O location.
3) ALE (Address Latch Enable) : This is an output signal used to give information regarding AD0-AD7 content. This is a positive going pulse generated every time when 8085 begins its operation.

   When ALE is high then the contents on AD0-AD7 are address A0-A7 & when ALE is low, then the contents on AD0-AD7 are data i.e. D0-D7.

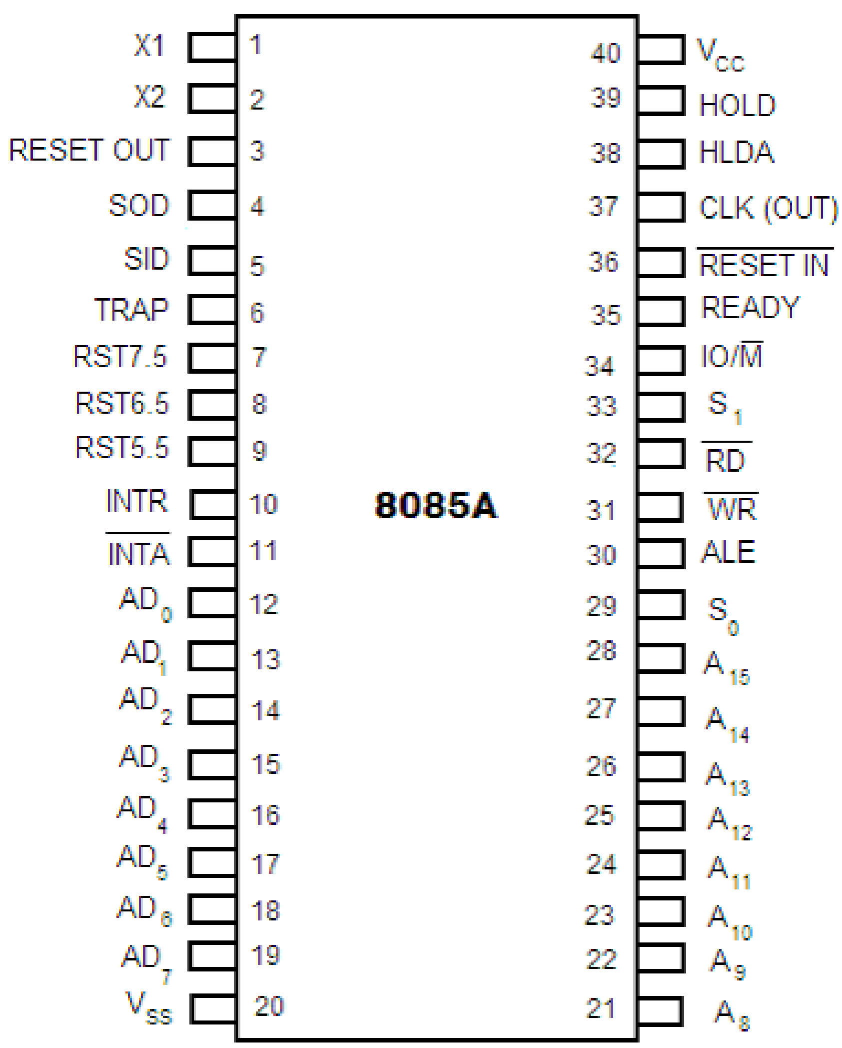


Figure 2.3 pin diagram of 8085

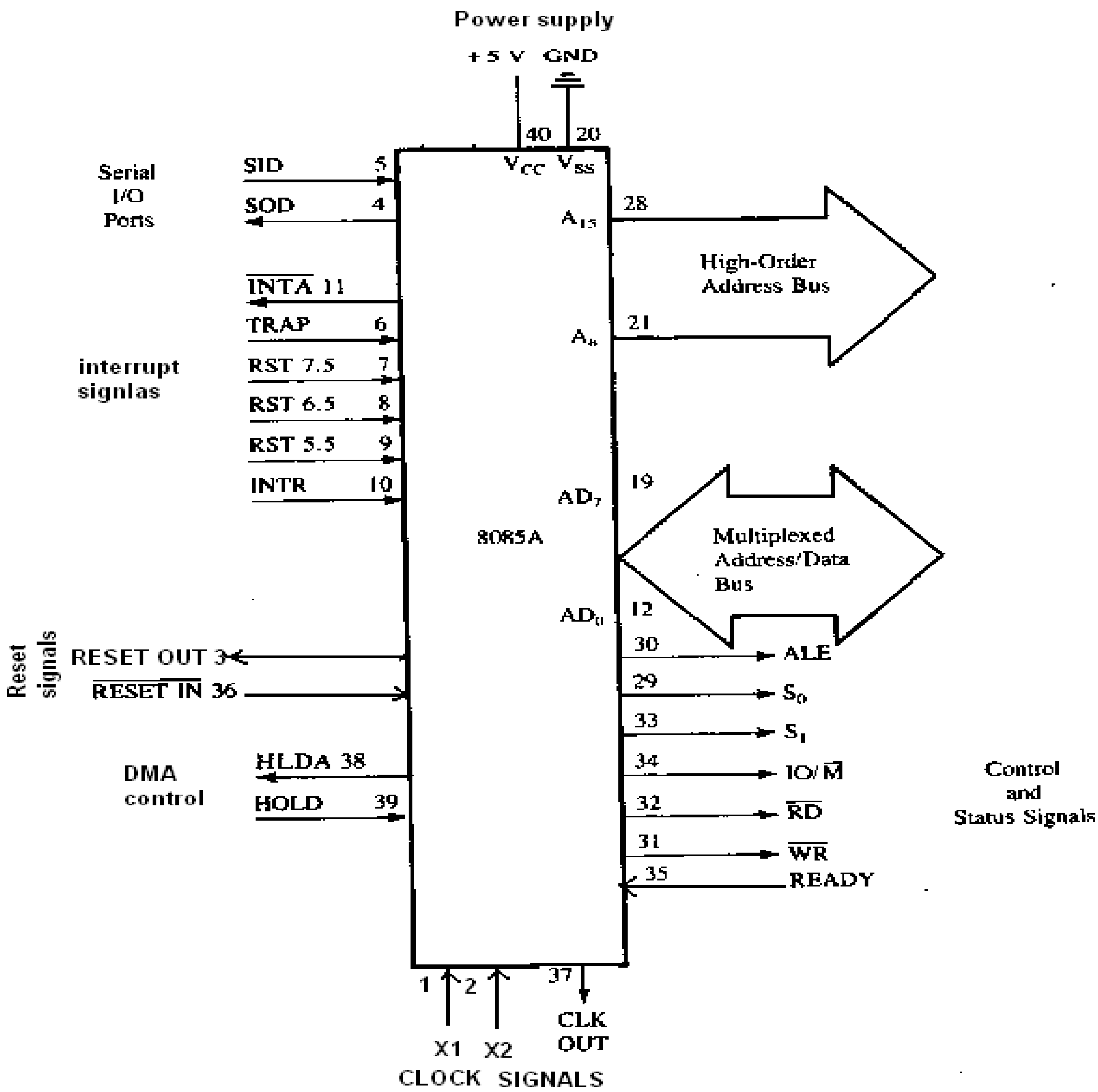


Figure 2.4 8085 signal diagram

Status signals:

1) IO/M: This is output status signal. It is used to differentiate between I/O & memory operations. When it is high it indicates an I/O operation (I/O devices are interfaced) & when it is low it indicates memory operation (memory chip is selected).
2) S0 & S1 (Output): These are status signals used to give information of operation performed by µp as shown in Table 2.1.

S0	S1	operation
0	0	Halt
0	1	Read
1	0	Write
1	1	Opcode fetch

Table 2.3

READY (Input):

If Ready is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If Ready is low, the CPU will wait for Ready to go high before completing the read or write cycle.

Clock Signals:

1) X1, X2 (Input): Crystal or R/C network is connected here to set the frequency of internal clock generator. The generated frequency is divided by 2 and then it is given to the various internal blocks for its operation.
2) CLK (Output): This is output signal where the internal operating frequency is available.

DMA control signals:

HOLD & HLDA: HOLD is active high input signal used by other controller to request µp about use of address and data lines. When µp receives this signal it sends HLDA as acknowledgement signal.

RESET signals:

1) RESET IN (Input): This is active low signal which is input to µp. It resets the µp & PC becomes 0000H. None of the other flags or registers (except the instruction register) are affected. The CPU is held in the reset condition as long as Reset is applied.
2) RESET OUT (Output): This is active low output signal which is used to indicate that µp is reset.

Interrupt controlled signals: The 8085 has 5 interrupt inputs: INTR, RST5.5, RST6.5, RST 7.5, and TRAP.

1) INTR (Input) & INTA (Output): Interrupt request & acknowledge. The INTR is an active high Interrupt. When µp receives an interrupt signal, it sends the active low interrupt acknowledgement i.e. INTA. This interrupt have least priority.
2) RST 7.5, RST6.5, RST5.5: (Restart interrupts): These are active high, vectored and maskable interrupts. Their vector locations are 003CH, 0034H, 002CH respectively.
3) TRAP (Input): This is active high. It is highest priority interrupt. It is a non- maskable interrupt. It is unaffected by any mask or Interrupt Enable. When the signal is received then PC goes to location 0024H.

Serial I/O control signal:

1) SID (Input): Serial input data line. The serial data from peripheral devices is inputted.
2) SOD (output): Serial output data line. The serial data is outputted from µp or to peripherals.

Power supply & frequency signals:

3) Vcc: +5 volt supply.
4) Vss: Ground Reference

2.4 8085 System Bus

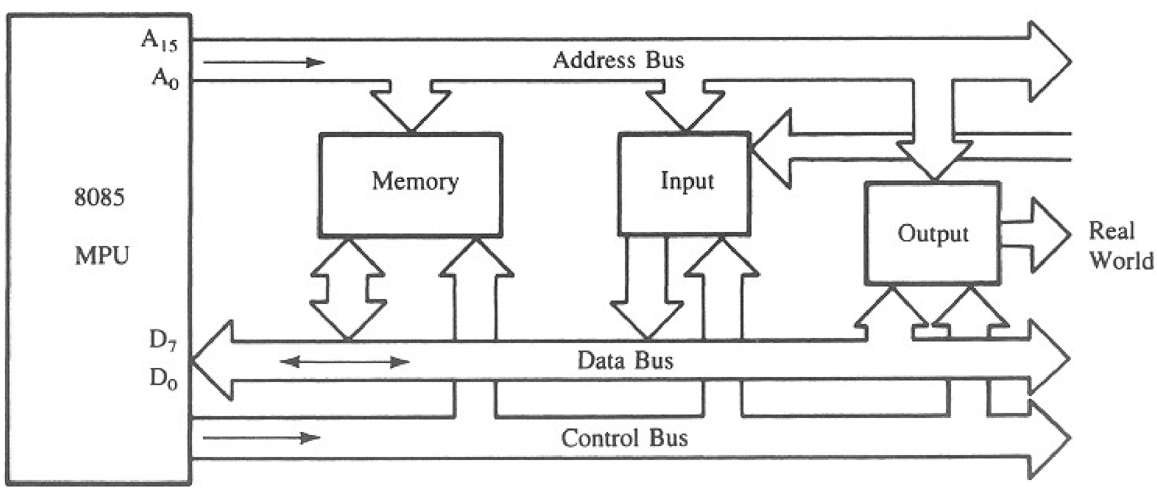


Figure 2.5 8085 bus structure

Bus means a group of lines used to transfer the bits between µp & peripheral devices or within different sections of µp. Typical system uses a number of buses (collection of wires) which transmit binary numbers, one bit per wire. A typical microprocessor communicates with memory and other devices (input and output) using three buses: Address Bus, Data Bus and Control Bus.

Address Bus:

The Address Bus is a group of 16 lines generally identified as A_0-A_{15}. Address bus is unidirectional, i.e. numbers only sent from microprocessor to memory, not other way. One address line identifies two locations means two registers each of 8 bit or 1-byte. Hence 16

address lines can identify 2^{16}=65536. The 8085µp have 16 address lines which is capable to locate 64KB memory locations. The address lines for 8085 µp are A_0, A_1, A_2, ----------, A_{14}, A_{15}, hence the addresses from 0000H to FFFFH which identify 64KB memory locations.

Data Bus:

It is a group of 8 lines. It is bidirectional, i.e. data (bits) may flow in any direction from microprocessor to peripherals & from peripherals to microprocessor. The 8 data lines enables the µp to manipulate 8 bit data ranging from 00H to FFH i.e.2^8=256. It determines the word length & register size of a µp. The word length of a data for 8085 is 8-bit hence 8085 is called 8-bit µp. Since data bus is 8 bits wide then largest number is 11111111 (255 in decimal). Therefore, larger number have to be broken down into chunks of 255. This slows microprocessor. Data Bus also carries instructions from memory to the microprocessor. Size of the bus therefore limits the number of possible instructions to 256, each specified by a separate number.

Control Bus:

The control bus comprised of various single lines that carry synchronization signals. The MPU uses these lines to send timing signals or pulses. The MPU generate specific control signals for every operation such as Memory Read [MEMR], Memory Write [MEMW], I/O Read [I/OR] etc.

2.5 8085 Programmable Registers:

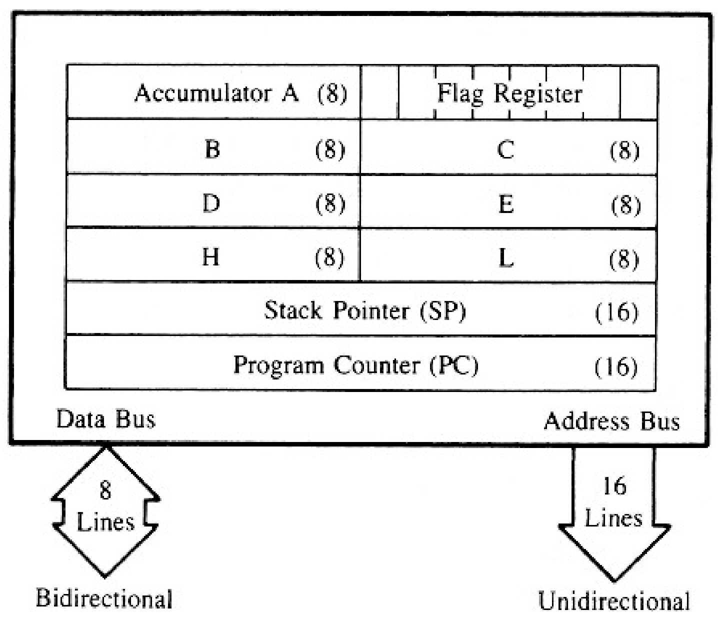


Figure 2.6 8085 registers

2.6 Reset Circuit :

In microprocessor, we provide power on reset and manual reset. When processor is reset by any way its program counter becomes 0000 and it will start its program from initial. RESET IN pin provided on 8085 will reset processor, when this pin is LOW for few msec and then reach to HIGH logic .This can be done using simple circuit as shown in fig. 2.7.

When power supply is switched ON, at time to capacitor will start charging exponentially and voltage across capacitor (to RESET PIN) remains 2.4 V up to t1 (voltage below 2.4 is treated as low for microprocessor) and hence t1-t0 is reset time. Then after t1, voltage across capacitor becomes more than 2.4 V and RESET pin becomes high. Value of R is 1KΩ to 10 KΩ and C is 1 to 10 microfarad .

When Switch parallel to capacitor is pressed, RESET pin becomes low and when released, it will become high. In this way it can be reset manually.

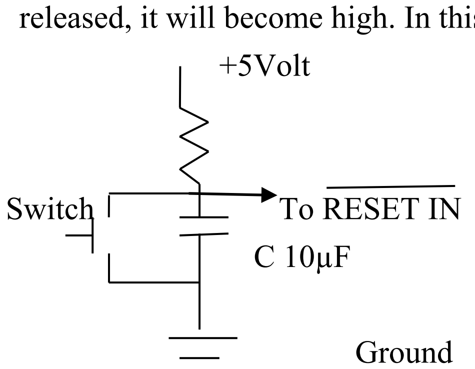


Fig 2.7 Reset Circuit

2.9 CLOCK Circuit

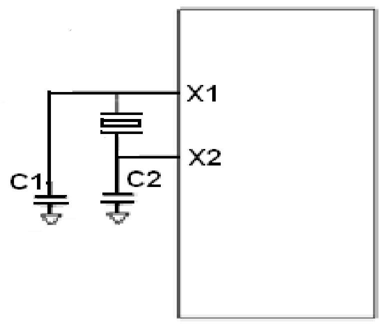


Fig 2.8 Clock Circuit

The two pins X1(1) and X2(2) are available to connect a crystal. The frequency is internally divided by two, therefore when a crystal of 6 MHz is connected then the clock pulses generated will be of 3 MHz. 8085 has on chip oscillator across the pin 1 and 2. Fig.2.8 shows crystal interface circuit. It will give stable frequency. Capacitor C1, C2 are used to avoid external noise

2.10 Demultiplexing of AD0-AD7 :

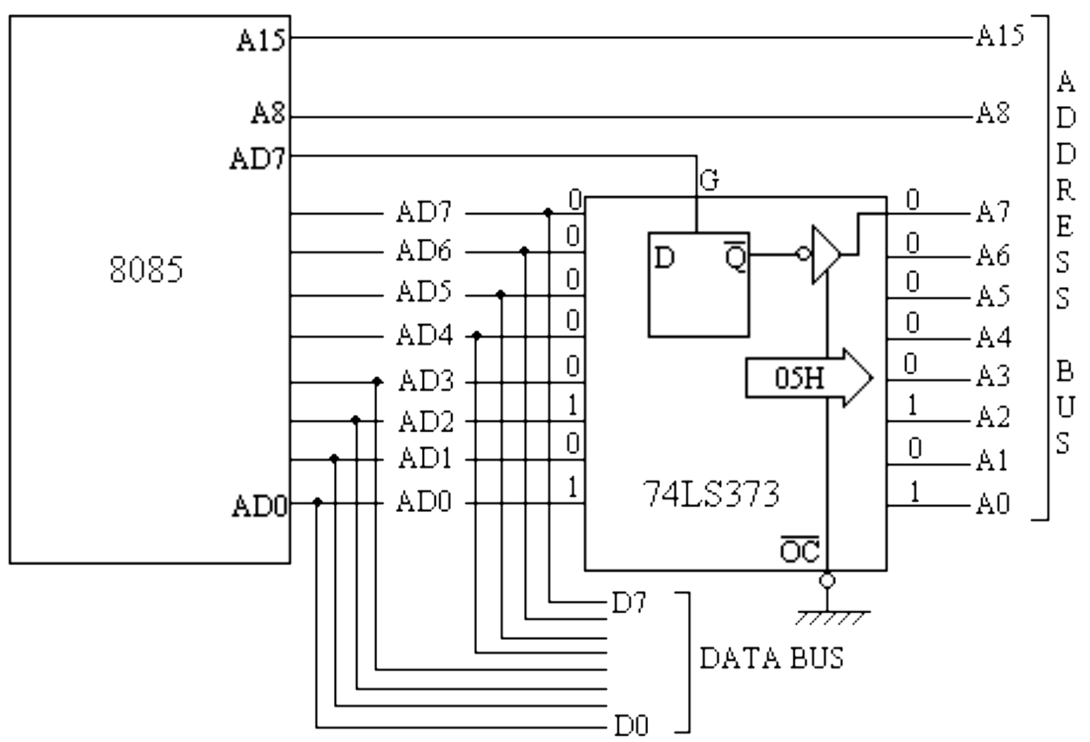


Fig 2.9 Demultiplexing of AD0-AD7

We know that the AD7– AD0 lines are serving a dual purpose and that they need to be demultiplex to get all the information.

The high order bits of the address remain on the bus for three clock periods. However, the low order bits remain for only one clock period and they would be lost if they are not saved externally. Also, notice that the low order bits of the address disappear when they are needed most.

To make sure we have the entire address for the full three clock cycles, we will use an external latch to save the value of AD7– AD0 when it is carrying the address bits. We use the ALE (Address Latch Enable) signal to enable this latch as shown in fig. 2.9.

During T1 the ALE goes HIGH. When ALE goes HIGH, the latch is enabled. So the o/p changes according to the i/p data. During T1 the o/p of latch is 05H. When ALE goes LOW, the data byte 05H is latched until the next ALE. And after the latching operation the o/p of the latch represents the lower order address bus A0-A7 and the AD7– AD0 lines can be used for their purpose as the bi-directional data lines.

2.11

2.12 8085 Machine Cycles:

The 8085 microprocessor has 5 (five) basic machine cycles as shownin Table 2.2

Machine cycle	Status signals			Control signals	
	IO/M	S1	S0	RD	WR
1. Opcode fetch cycle (4T)	0	1	1	0	1
2. Memory read cycle (3 T)	0	1	0	0	1
3. Memory write cycle (3 T)	0	0	1	1	0
4. I/O read cycle (3 T)	1	1	0	0	1
5. I/O write cycle (3 T)	1	0	1	1	0

Table 2.4 8085 Machine Cycles

2.13 Stack Memory:

The stack is the reserved area of the memory which is shared by microprocessor and programmer. The higher order address of RAM area is reserved as a stack. The 16 bit register which is holding the memory address of the stack is called a stack pointer. Programmer can use the stack to store the data which can be quickly accessed. The intermediate results and register contents can be stored onto the stack. Microprocessors use the stack during CALL and RET instructions. Whenever the CALL instruction is executed, the address of the next instruction is loaded onto the stack and subroutine is executed. Since every subroutine ends with RET instruction, so when RET instruction is executed, the program counter (PC) is loaded back with the address from the stack and now program execution starts from the location next to where it was called from.

The programmer can initialize the stack pointer by using the instruction LXI SP, XXXX H. e.g. LXI SP, 7000H, Then storing of Data begins from 6FFFH, means one less than 7000H.The data can be loaded or retrieved from the Stack using PUSH, POP instructions. When the information is written onto the stack, the operation is called as PUSH. When the information is read from the stack the operation is called as POP. The stack memory has the structure called as last in first out (LIFO) or first in last out (FILO).

2.13 Timing diagrams:

A timing diagram of an instruction is a graphical representation of the time taken by the µP to fetch, decode and execute an instruction. The size of the instruction and the frequency of the µP decide the total amount of time taken to execute an instruction.

1) **Instruction cycle:** Time required for completing the execution of an instruction is known as instruction cycle. The 8085 instruction cycle consists of one to six machines cycles for operations.
2) **Machine cycle:** It is the time required for completing a single operation. This operation can be accessing memory for read/write operation or accessing I/O device. There can be 3 to 6 clock periods or T-states in a machine cycle.
3) **T-states or clock cycles/periods (CLK):** T-state is equivalent to one clock period. It is the time in which only a subdivision of the operation can be performed. The total number of T-states determines the size of the machine cycle required to perform an operation.

   For Ex: If the internal clock frequency of 8085 microprocessor is 3 MHZ,

   One T-state 1/3 MHz =0.333 s= 0.333 x10-6 sec=333x10-9sec. (333 nano seconds nearly)

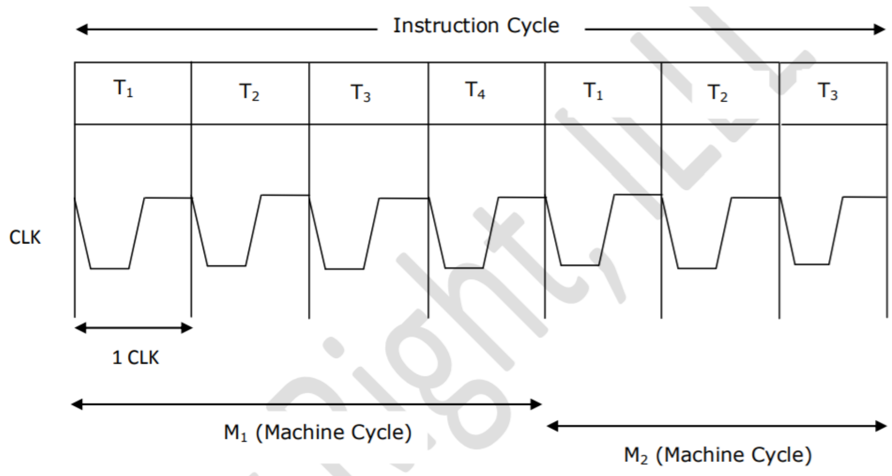


Fig:2.10 Timing Intervals

Note: If an instruction is one byte long only one machine cycle is required to fetch, decode and execute an instruction. e.g. MOV, ADD, SUB, ANA, ORA, RAR. Since the operands are in general purpose registers, decoding and executing requires only one clock cycle T4.

If an instruction is two byte or three byte long it requires more machine cycles. The 1st machine cycle M1 is for fetching the opcode from memory and subsequent machine cycles M2, M3 are required to read the data or address from memory or I/O devices and to write data in memory or I/O devices.

Timing diagram of MOV Instruction:

Ex. Timing diagram of MOV B, C instruction

Memory address	Mnemonics	Hex codes	Comment
2000 H	MOV B, C	41 H	; Copies the contents of the source register C into the destination register B. ;instruction MOV B, C is of 1 byte; therefore the complete instruction is stored in a single memory address

It is an one byte instruction and requires only one machine cycle(M1) to fetch, decode and execute an instruction.

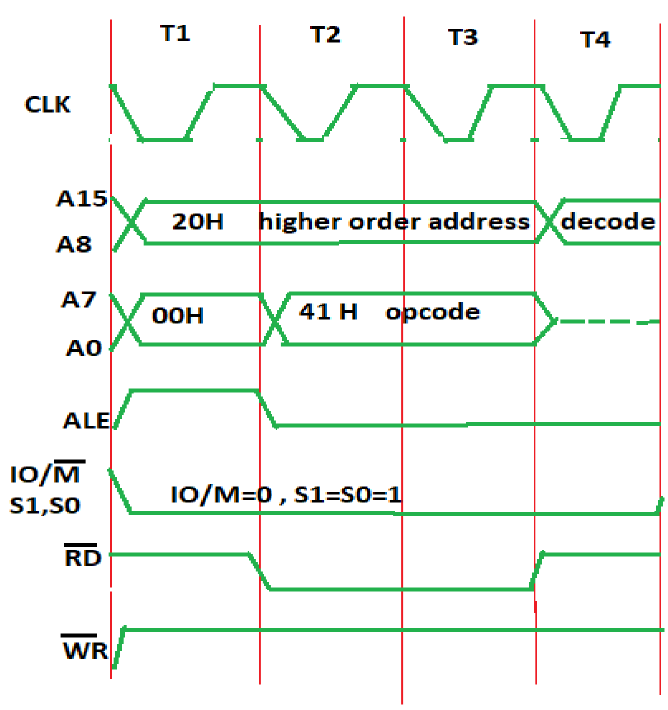


Fig:2.11 Timing diagram of MOV Instruction

During 1st clock cycle T1, the microprocessor issues a low IO/M signal to indicate that it wants to make communication with memory. Again it sends S_1 and S_0 signals to be high to indicate that it is going to perform fetch operation. Microprocessor sends high order memory address 20H on the address lines A8-A15 and low order address 00H on the lines AD0-AD7. Also it sends ALE signal high to latch low order memory address.

During T2, AD0-AD7 becomes ready to carry the data. In T2 microprocessor makes RD low so that the specified memory location is enabled and opcode 41H from it is now available on data bus.

During T3, the opcode is placed in Instruction Register (IR). The memory is disabled by making RD high. Thus here the fetch cycle is completed.

The opcode is decoded in T4.

Timing diagram of MVI Instruction:

Ex. Illustrate the execution of two byte instruction **MVI B, 25 H** stored at locations as follows:

Memory address	Mnemonics	Hex codes	Comment
6000 H	MVI B, 25H	06 H	; copy the specified data into destination register B
6001 H		55 H	; It is a 2 byte instruction; therefore the complete instruction is stored in a two memory locations

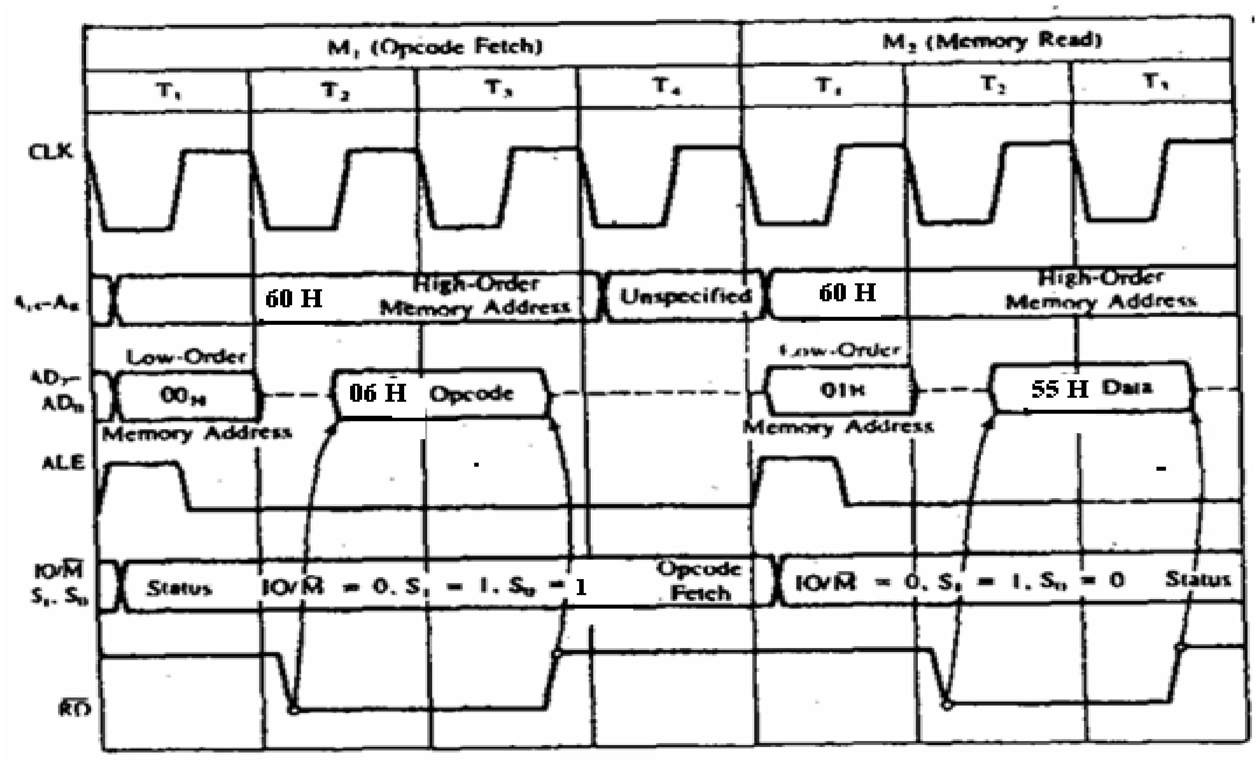


Fig:2.12 Timing diagram of MVI Instruction

This instruction requires two machine cycles for its complete execution: M1—opcode fetch and M2—memory read. M1 consists of 4 T-states and M2 consists of 3 T-states.

<u>1] M1-Opcode fetch cycle</u>

T1-state: a) Microprocessor issues IO/M=0, S1=1, S0=1.

b) Microprocessor places high order address 60H on the lines A8-A15 and low order address 00H on the lines AD0-AD7. Also microprocessor makes ALE signal high.

T2-state: Microprocessor sends RD to enable the memory location. So now the opcode 06 H is available on data bus.

T3-state: The opcode 06 H is read and placed in IR.

T4-state: The opcode is decoded.

<u>2] M2-Memory Read Cycle:</u>

i)T1-state: a) Microprocessor issues S1=1, S0=0, IO/M=0

b) Microprocessor places high order address 60H on the lines A8-A15 and low order address 01H on the lines AD0-AD7. Also microprocessor makes ALE signal high.

T2-state: Microprocessor sends RD to enable the memory location. So now the data 55 H is available on data bus.

T3-state: The data on data bus is now transferred into accumulator.

Ex. Illustrate the execution of two byte instruction **MVI B, 43 H** stored at locations as follows:

Memory address	Mnemonics	Hex codes	Comment

2000 H	MVI B, 43H	06 H	; copy the specified data into destination register B
2001 H		43 H	; It is a 2 byte instruction; therefore the complete instruction is stored in a two memory locations

This instruction requires two machine cycles for its complete execution: M1—opcode fetch and M2—memory read. M1 consists of 4 T-states and M2 consists of 3 T-states.

1] M1-Opcode fetch cycle

T1-state: a) Microprocessor issues IO/M=0, S1=1, S0=1.

b) Microprocessor places high order address 20H on the lines A8-A15 and low order address 00H on the lines AD0-AD7. Also microprocessor makes ALE signal high.

T2-state: Microprocessor sends RD to enable the memory location. So now the opcode 06 H is available on data bus.

T3-state: The opcode 06 H is read and placed in IR.

T4-state: The opcode is decoded.

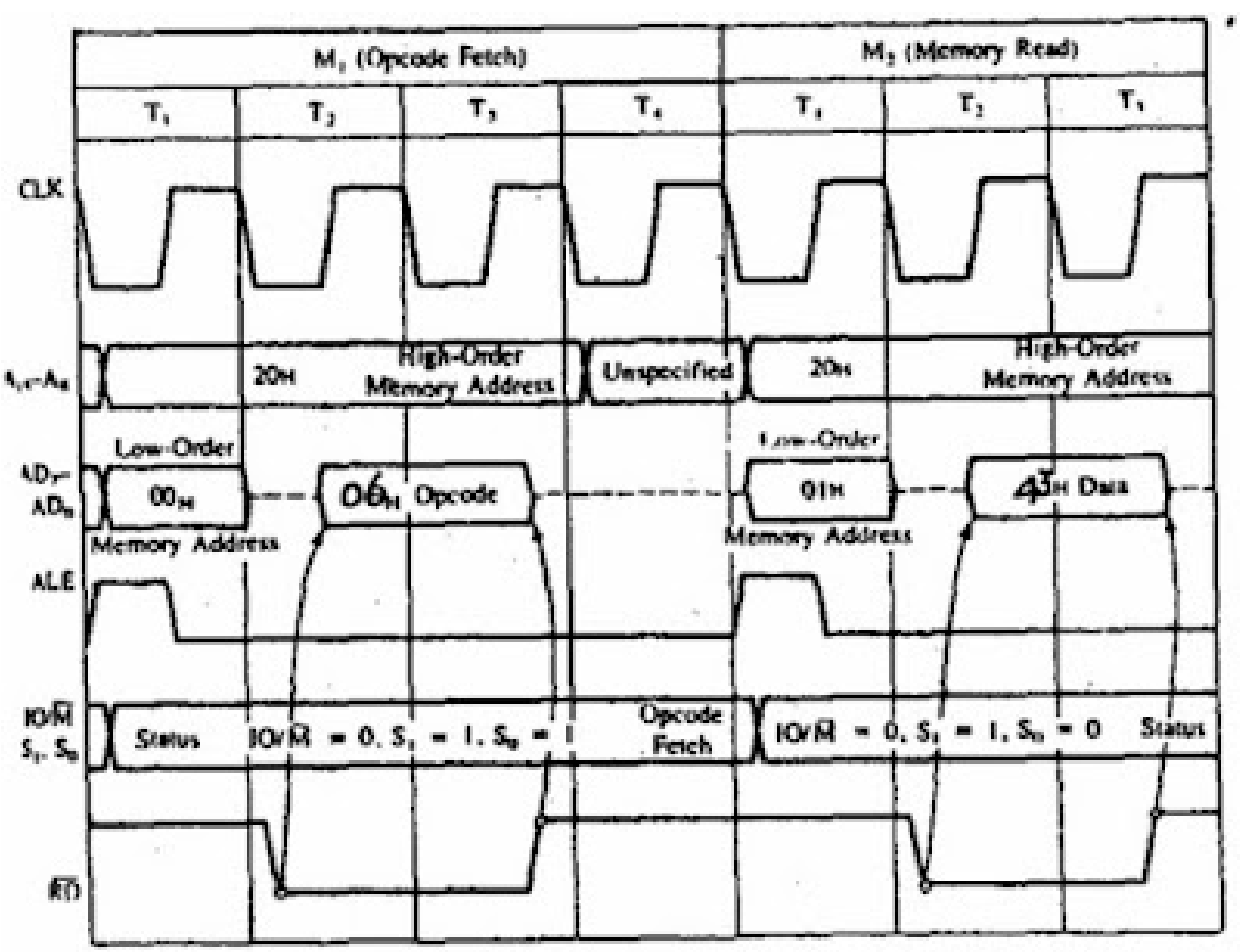
2] M2-Memory Read Cycle:

i)T1-state: a) Microprocessor issues S1=1, S0=0, IO/M=0

b) Microprocessor places high order address 20H on the lines A8-A15 and low order address 01H on the lines AD0-AD7. Also microprocessor makes ALE signal high.

T2-state: Microprocessor sends RD to enable the memory location. So now the data 43 H is available on data bus.

T3-state: The data on data bus is now transferred into accumulator.



Exercise:

Select correct alternatives:

1) 8085µp is------------------ bit microprocessor.

a) 4 b) 8 c) 16 d) 32

2) Operating frequency of 8085µp is------------------ MHz

a) 1 b) 2 c) 3 d) 4

3) technology is used to fabricate 8085µp.
   a) NMOS b) CMOS c) HMOS d) TTL
4) register is used to indicate status of the result.
   b) ACC b) Flag c) PC d) SP
5) is a 16 bit register.
   a. ACC b) Flag c) PC d) B
6) is a memory pointer register.
   b. ACC b) Flag c) PC d) B
7) ------ signal is used to Demultiplexing AD0-AD7.
   a. RESET IN b) ALE c) S0, S1 d) IO/M
8) 8085 microprocessor can access -----------------bytes of memory.
   a) 8 K b) 16K c) 32K d) 64K
9) 8085 microprocessor has------ bit data bus.
   a) 4 b) 8 c) 16 d) 32
10) To communicate with slower memories-------- signal is used.
   a) RESET IN b) ALE c) READY d) HOLD
11) Stack memory is initialized using------- instruction.
   a) LXI H, xxxxH b) LXI SP, xxxxH c) PUSH B d) POP B
12) are 16-bit registers.
   a) PC and ACC b) SP and ACC c) PC and SP d) ACC and B
13) is not be an Interrupt signal.
   a) INTR b) RST 7.5 c) RST 5.5 d) HOLD
14) Principal register in 8085 microprocessor is------
   a) ACC b) Flag c) PC d) SP
15) registers can be acts as inputs for ALU.
   a) ACC and B b) B and C c) PC and SP d) ACC and Temp Register
16) registers are not user accessible.
   a) ACC and B b) B and C c) PC and SP d) W and Z
17) 8085 microprocessor has ------ number of General purpose registers.
   a) 4 b) 6 c) 8 d) 10
18) 8085 microprocessor has ------bit address bus.
   a) 4 b) 8 c) 16 d) 32
19) 8085 microprocessor can be reset by using the-------- signal.
   a) HOLD b) ALE c) READY d) RESET IN
20) If crystal of 6MHz is connected to Microprocessor then the operating clock frequency is ---------MHz
   a) 6 b) 3 c) 16 d) 1
21) Microprocessor writes a data into a memory by activating the signals as--------
   a) S0=0, S1=0, IO/M=1, RD=0
   b) S0=0, S1=0, IO/M=0, RD=0
   c) S0=0, S1=1, IO/M=0, WR=0
   d) S0=1, S1=0, IO/M=0, WR=0
22) Microprocessor reads a data from input device by activating the signals as--------
   a) S0=0, S1=0, IO/M=1, RD=0
   b) S0=0, S1=0, IO/M=0, WR=0
   c) S0=0, S1=1, IO/M=0, WR=0
   d) S0=0, S1=1, IO/M=1, RD =0
23) signal is not an output signal.
   a) RD b) WR c) S0 d) READY
24) Microprocessor uses ------signals to communicate with serial devices.
   a) HOLD and HLDA b) TRAP and RST 7.5
   c) SID and SOD d) READY and HOLD
25) Addressing capacity of microprocessor depends upon ----- --.
   a) address lines b) data lines

c) control lines d) all of these

26) 8085 microprocessor has primarily --------- interrupt signals.
a) 4 b) 5 c) 8 d) 10

27) The 8085 microprocessor uses--------signals to share system bus with Direct Memory Access (DMA) controller.
a) HOLD and HLDA b) TRAP and RST 7.5
c) SID and SOD d) READY and HOLD

28) The stack memory has -------- type of operational structure.
a) LIFO b) FILO c) LILO d) both a and b

29) ------------ is a non maskable interrupt
a) RST 7.5 b) RST5.5 c) TRAP d)INTR

30) The interrupt having specific address in the memory is called as ----------------
a) software interrupt b) vectored interrupt
c) hardware interrupt d) maskable interrupt

31) ----- is a edge triggered interrupt
a) RST7.5 b) RST 6.5 c) INTR d) RST 5.5

32) -----instruction is used to send a data in serial communication
a) SIM b) SUB c) SBB d) RIM

33) In 8085---------- is having highest priority
a) RST 7.5 b) TRAP c) INTR d) INTA

34) The interrupt that can be ignored is called as ------
a) Non maskable interrupt b) Maskable interrupt
c) Hardware interrupt d) Vectored interrupt

Long Answer questions:

Q. Draw an internal architecture of 8085 Microprocessor and explain it's various blocks.
Q. Draw the signal diagram of 8085 Microprocessor and explain various signals.
Q. Draw the pin diagram of 8085 Microprocessor and explain various signals.
Q. Draw the timing diagram of MOV A, B operation and explain it.
Q. Draw the timing diagram MVI A, 25H operation and explain it.

Short Answer questions:

Q. Explain Flag register of 8085 Microprocessor.
Q. Explain Stack and Stack pointer register.
Q. Explain 8085 programmable registers.
Q. Write a note on Clock and Reset circuits.
Q. What is ALE? Explain the functions of ALE in 8085.
Q. How AD_0-AD_7 bus is demultiplexed?

Answers: Select correct alternatives:

1.b 2.c 3.a 4.b 5.c 6.c 7.b 8.d 9.b 10.c

11.b 12.c 13.d 14.a 15.d 16.d 17.b 18.c 19.d 20.b

21.d 22.d 23.d 24.c 25.a 26.b 27.a 28.d

29.c 30. b 31.a 32.a 33. B 34.b