Chapter.....3

LOGIC FAMILIES

3.1 INTRODUCTION

Logic gates are constructed using different active devices such bipolar junction transistor or filed effect transistor. With the invention of modern technology of component fabrication over a small size silicon chip, it became possible to integrate more number of components over a specific chip space. Such circuits are known as IC's .The density of components in an IC is indicated by a scale known as *Scale of Integration.* In the Table 3.1 difference scales of integration are shown.

Table 3.1: Scale of Integration

Scale of integration	Number of logic Gates
1) Small Scale Integration (SSI)	< 12
2) Medium scale Integration (MSI)	12to 99
3) Large Scale Integration (LSI)	100 To 999
4) Very large Scale Integration (VLSI)	1000 To 9999
5) Ultra large scale Integration (ULSI)	> 10000

Groups of compatible IC's with same logic levels and supply voltages have been fabricated using specific circuit configuration that performs various logic functions, known as Logic Families of digital IC's.

3.2 TYPES OF LOGIC FAMILIES

Two basic technologies for manufacturing digital IC'S are

1. Unipolar technology that gives rise to Unipolar Logic Family
2. Bipolar technology that gives rise to Bipolar Logic Family

1) Unipolar Logic Family

The Logic Family in which Unipolar Active Devices such as MOSFET (Metal Oxide Semiconductor Field Effect Transistor) are used in building the Logic Gates is known as Unipolar Logic Family. Further it has following members-

1. PMOS (P-channel MOSFET) Family
2. NMOS (N-channel MOSFET) Family
3. CMOS (Complementary MOSFET) Family

2) Bipolar Logic Family

The Logic Family in which Bipolar Active Devices such as Semiconductor Diodes and Bipolar Transistors are used in building the Logic Gates is known as Bipolar Logic Family. This is further classified as *Non-Saturated* and *Saturated* Logic Families.

Saturated Logic Family has members as shown in Table 3. 2.

Table 3.2: Types of TTL Logic Family

1.	Resistor-Transistor Logic	[RTL]
2.	Direct Coupled Transistor Logic	[DCTL]
3.	Integrated Injection Logic	[IIL or I^2L]
4.	Diode Transistor Logic	[DTL]
5.	High Threshold Logic	[HTL]
6.	Transistor Transistor Logic	[TTL]

Non-Saturated Logic Family has following members-

1. Schottky TTL
2. Emitter coupled logic (ECL)

3.3 CHARACTERISTICS OF DIGITAL IC'S (LOGIC FAMILIES)

To use digital IC's efficiently in the system designing, manufacturers provide some technical information along with other characteristics known as s*pecifications*. The various characteristics of digital IC's are:

1. *Propagation delay. (Speed of operation)*
2. *Power dissipation*
3. *Figure of Merit*
4. *Fun-In /Fan-out*
5. *Current and Voltage parameters*
6. *Noise-Immunity*
7. *Operating-Temperature*

1. Propagation Delay Time (t_p)

Most of the digital device such as logic gates does not respond instantaneously to the input signals. There exists a time lag between change in input and change in output to a specific level. This is known as propagation delay time. It is defined as-

The time required to change the output from one logic state to another after input is applied.

Propagation delay time for low to high switching or high to low switching is practically not equal. Hence there average value is stated as

$$t_P = \frac{t_{PLH} + t_{PHL}}{2} \quad (\mu S)$$

Where t_{PLH} = Propagation delay time for low to high transition
t_{PHL} = Propagation delay time for high to low transition

These delay times are calculated between 50 % voltage levels of input and output as shown in Fig.3.1.

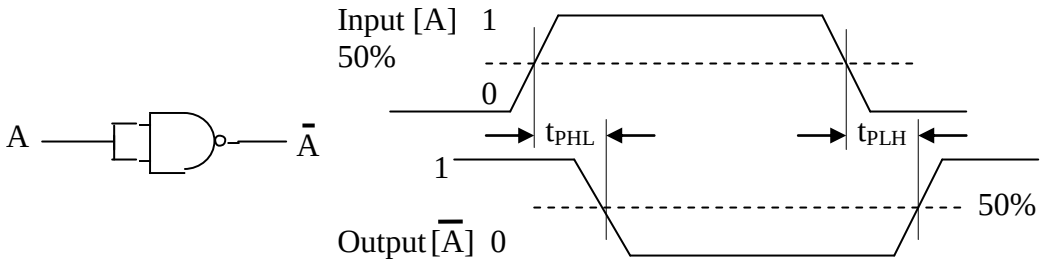


Fig 3.1: Measurement of Propagation delay time

Higher the propagation delay time lower will be speed of operation and vice versa. Typically for TTL family it is of the order of *10 nsec.*

2. Power dissipation:

All logic circuits need DC power for their operation. When DC voltage is applied the IC draws some amount of current from the DC source. In other words digital ICs consume power, which is dissipated in from of heat. The power dissipation is defined as *"The product of voltage applied and current drawn by the digital IC"*

$$P_D = V_{CC} \times I_C$$

The logic gate draws different currents when the output is low or high. Therefore average power dissipation is stated as-

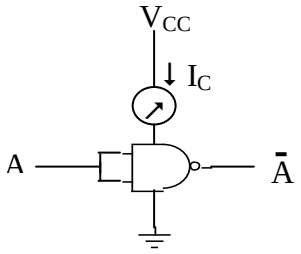


Fig. 3.2: Power Dissipation

$$P_D = \frac{P_{DL} + P_{DH}}{2} \quad (mW)$$

Most of the digital IC's draw the current in the range of milliampere. Hence power dissipation specified in terms milliwatts. Smaller the power dissipation better is the quality of digital IC.

3. Figure of Merit :

If internal resistance of logic gate is increased, its power dissipiation smaller, however this would increase propagation delay time. Both of these factors are expressed in terms of a factor called as Figure of Merit. It is defined as- *"The product of power dissipation and propagation delay time."*

i.e. $FoM = t_p \times P_D$

Generally it is stated in Pico-Joule (pJ). Smaller the value of FoM better is Quality of digital IC.

4. Fan-In/Fan-Out:

Fan-In

Number of inputs available with a logic gate is known as its Fan-In. This is decided by the design aspects of logic gates. Higher Fun-In provides more flexibility in the circuit designing.

E.g. the gates have Fan-In of 2, 3, 4 & 8 respectively.

Fan-Out

In designing a digital system one gate has to drive one or more gates as shown in figure 3.3

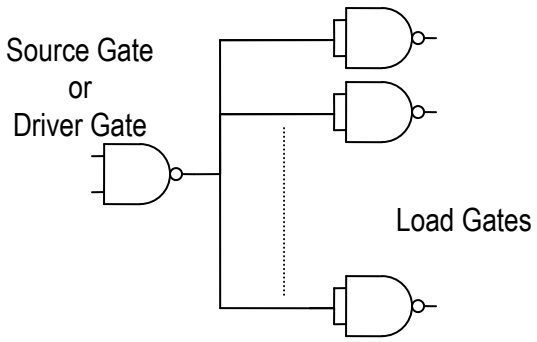


Fig.3.3: Concept of Fan out

Fan-Out is the maximum number of load gates from the same Logic Family that can be driven reliably by a source or driver gate.

This number indicates the driving capacity of a logic gate Hence it is also known as *Loading Factor*.

Fan-Out is calculated as

$$\text{Fan-out} = \frac{I_{0L}}{I_{IL}} = \frac{I_{OH}}{I_{IH}}$$

Higher the Fan-out better is the family. For TTL Gate it is typically 10, whereas for C-MOS family it is 50 or more.

5. Current and Voltage Parameters:

Voltage parameters: Any logic family has following voltage parameters
[Values stand for TTL]-

1) V_{IH} = High Level Input Voltage [2.0 V]
It is the minimum Input voltage that is recognized by gate as logic '1'.
2) V_{IL} = Low Level Input Voltage [0.8 v]
It is the maximum Input voltage that is recognized by gate as logic '0'.
3) V_{OH}= High Level Output Voltage [2.4 V]
It is the minimum Output voltage that is recognized by gate as logic '1'.
4) V_{OL} = High Level Output Voltage [0.4 V]
It is the maximum Output voltage that is recognized by gate as logic '0'.
Input and output voltage profiles are shown in Fig.3.4 (a) and Fig.3.4 (b) .

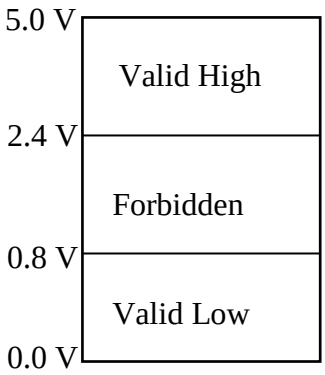


Fig. 3.4 (a) Input Profile

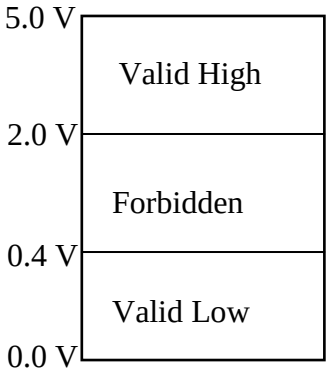


Fig. 3.4 (b) Output Profile

Current parameters:

1. I_{IH}= High Level Input Current [40 μA]
   It is the minimum current, which must be supplied by source at logic '1'.
2. I_{IL}=Low Level Input Current [1.6 mA]
   It is the minimum current, which must be supplied by source at logic '0'.
3. I_{OH} = High Level Output Current [400 μA]
   It is the maximum current, that gate can source (supply) at logic '1'.
4. I_{OL} = Low Level Output Current [16 mA]
   It is the maximum current, that gate can sink (take in) at logic '0'.
5. I_{cc} (1) = High Level Supply Current
   It is the maximum supply current drawn by gate [or Digital IC] when the output is at logic '1'.
6. Icc (0) = High Level Supply Current
   It is the maximum supply current drawn by gate [or Digital IC] when the output is at logic '0'.

6. Noise Immunity and Noise Margin:

Noise is an external signal other than signal meant for device. This may be generated by vehicle ignition or current through nearby witting or device itself. Such noise tends to trigger the logic circuit in undesirable manner. All logic families have ability to tolerate such a noise to a certain extent. This ability to tolerate the noise is known as *Noise Immunity*.

In other words the maximum noise voltage a logic device can withstand or tolerate without making false change in the output is called as noise immunity and quantitative measure of noise immunity is known as *Noise Margin*.

It is given by,

$$\text{Noise Margin} = V_{OH} - V_{IH} \quad \text{(for logic '1')}$$
$$= 2.4 - 2.0 = \mathbf{0.4\ V} \text{ for TTL}$$
$$\text{Noise Margin} = V_{IL} - V_{OL} \quad \text{(for logic '0')}$$
$$= 0.8 - 0.4 = \mathbf{0.4\ V} \text{ for TTL}$$

7. Operating temperature:

Semiconductor devices are strongly temperature dependent. They are to be operated within the safe range of temperature. This range is generally specified by manufacturers of digital IC's.

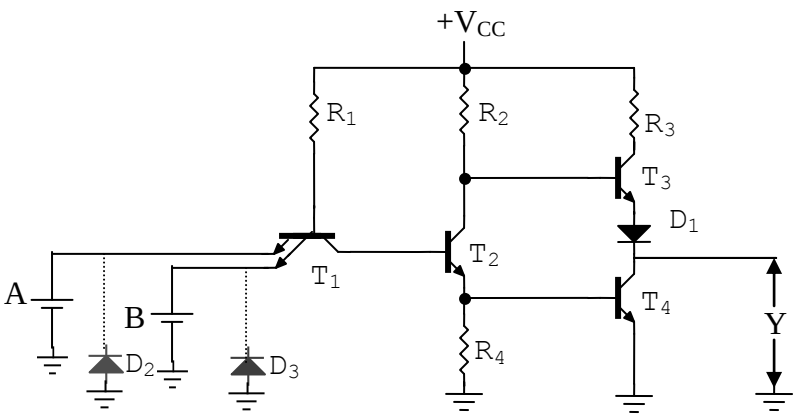
Logic Families used in industrial and communication applications; the temperature range is 0^0C to 70^0C (74XX Series), whereas for military applications, it ranges from -55^0C to 125^0C (54XX series).

3.4 TTL (TRANSISTOR-TRANSISTOR LOGIC) TECHNOLOGY

Because of particular characteristics, TTL technology is more popular in digital IC's. In this technology transistors are used as a main active device. This family has five major members as given in Table 3.1.

3.4.1 TTL-NAND GATE

Output is high when any or all inputs are low is the logic for NAND Gate. It is a universal building block of digital system. It is widely available in standard IC form. In its



simplest form it is shown in the Fig.3.5.

Fig.3.5: TTL NAND Gate

Transistor T_1 is multiple emitter input transistor and it is an input transistor. Its collector voltage goes to transistor T_2. This transistor drives the totem pole pair of transistors. Output is taken at collector of T_4. The transistor pair consisting of T_3 (Emitter Follower) and T_4 (CE-Transistor) forms the Totem-Pole output stage. This stage has following advantages-

1. It provides low output impedance in both the cases i.e. when output is high or low.
2. Since output impedance is low it provides high switching rate i.e. high speed of operation

Working

The working of TTL NAND gate can be explained in four cases as-

Case-1: A=0, B=0

With both the inputs low, transistor T_1 saturates and its collector voltage goes low. This keeps the transistor T_2 OFF. High collector voltage of T_2 turns transistor T_3 ON. As there is no current through R_4, transistor T_4 gets no base bias and hence it remains OFF. Output Y therefore goes high.

Case-2: A=0, B=1

With input A grounded (low) transistor T_1 conducts. Its collector voltage goes low. This keeps the transistor T_2 OFF. High collector voltage of T_2 turns transistor T_3 ON. As there is no current through R_4, transistor T_4 gets no base bias and hence it remains OFF. Output Y therefore goes high.

Case-3: A=1, B=0

With input B grounded (low) transistor T_1 conducts. Its collector voltage goes low. This keeps the transistor T_2 OFF. High collector voltage of T_2 turns transistor T_3 ON. As there is no current through R_4, transistor T_4 gets no base bias and hence it remains OFF. Output Y therefore goes high.

Case-4: A=1, B=1

With both inputs high, emitter junctions of T_1 are reverse biased. It goes to OFF state. The high collector voltage of T_1 turns transistor T_2 ON. The transistor T_3 remains OFF, as collector voltage of T_2 is low. The voltage drop across R_4 makes the base of T_4 high enough to turn T_4 ON. Output Y therefore goes low.

The action is summarized in Truth table. as shown in Table 3.3.

Table 3.3: Truth-Table of NAND Gate

Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Role of D_1

In case of totem pole output pair of transistors if T_3 is ON, T_4 should remains OFF and vise versa. However when T_4 is ON the collector voltage of T_2 will be-

$$V_{BE4}+V_{CE2} = 0.7 + 0.2 = 0.9 \text{ V}$$

In the absence of diode D_1 this voltage easily turns the T_3 ON. The presence of diode D_1 increases a turn on voltage of T_3 to 1.4V. This is more than 0.9 V. This ensures that the transistor T3 remains OFF when T_4 is ON.

Diodes D2 and D3 are used to avoid ringing during fast switching. These are also called as clamping diodes.

3.4.2 TTL-NOR GATE

Output is high when all inputs are low is the logic for NOR Gate. It is another universal building block of digital system. It is widely available in standard IC form. In its simplest form it shown in the Fig. 3.6.

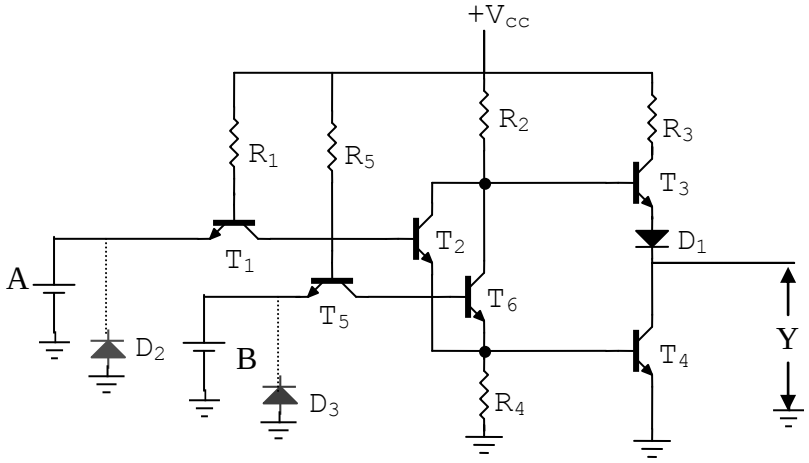


Fig. 3.6: TTL NOR Gate

Transistors T_1 & T_2 forms input A and transistors T_5 & T_6 forms input B. Its collector voltage of T_1 goes to transistor T_2, while collector voltage of T_5 goes to transistor T_6. Transistors T_2 & T_6 are in parallel. Their collector voltage drives the transistor T_3 and their current flows through R_4 that develops base voltage for T_4. These transistors thus drive the totem pole pair of transistors. Output is taken at collector of T_4.

Working

The working of TTL NOR gate can be explained in four cases as-

Case-1: A=0, B=0

With both the inputs low, transistor T_1 & T_5 saturate and their collector voltages go low. This keeps the transistor T_2 & T_6 OFF. High collector voltage of T_2 & T_6 turns transistor T_3 ON. As there is no current through R_4, transistor T_4 has no base bias and hence it remains OFF. Output Y therefore goes high.

Case-1: A=0, B=1

With inputs B high, transistor T_5 gets OFF and its collector voltage goes high. This keeps the transistor T_6 ON. Low collector voltage of T_6 turns transistor T_3 OFF. As there is current through R_4, transistor T_4 has sufficient base bias and hence it gets ON. Output Y therefore goes low.

Case-3: A=1, B=0

With inputs A high, transistor T_1 gets OFF and its collector voltage goes high. This keeps the transistor T_2 ON. Low collector voltage of T_2 turns transistor T_3 OFF. As there is current through R_4, transistor T_4 has sufficient base bias and hence it gets ON. Output Y therefore goes low.

Case-4: A=1, B=1

With inputs high, transistor T_1 & T_5 get OFF and their collector voltages go high. This keeps the transistors T_2 & T_6 ON. Low collector voltage of T_2 & T_6 turns transistor T_3 OFF. As there is current through R_4, transistor T_4 has sufficient base bias and hence it gets ON. Output Y therefore goes low.

The action is summarized in truth table as shown in Table 3.4.

Table 3.4: Truth Table of TTL NOR Gate

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

3.4.3 TTL-NOT Gate [Inverter]

Output is high when input is low and vice versa is the logic for NOT Gate. In its simplest form it is shown in the Fig.3.7.

Transistor T_1 is input transistor. Its collector voltage goes to transistor T_2. This transistor drives the totem pole pair of transistors. Output is taken at collector of T_4. The transistor pair consisting of T_3 (Emitter Follower) and T_4 (CE-Transistor) forms the Totem-Pole output stage.

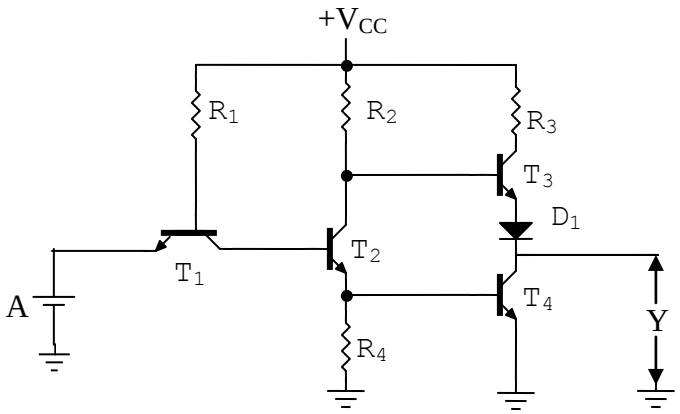


Fig.3.7: TTL NOT Gate

Working

The working of TTL NOT gate can be explained in two cases as-

Case-1: A=0

With input A low, transistor T_1 saturates and its collector voltage goes low. This keeps the transistor T_2 OFF. High collector voltage of T_2 turns transistor T_3 ON. As there is no current through R_4, transistor T_4 gets no base bias and hence it remains OFF. Output Y therefore goes high.

Case-2: A=1

With input A high, emitter junction of T_1 are reverse biased. It goes to OFF state. The high collector voltage of T_1 turns transistor T_2 ON. The transistor T_3 remains OFF, as collector voltage of T_2 is low. The voltage drop across R_4 makes the base of T_4 high enough to turn T_4 ON. Output Y therefore goes low.

The action is summarized in Truth table as shown in Table 3.5.

Table 3.5: Truth Table of TTL NOT Gate

Input	Output
A	Y
0	1
1	0

3.5 OPEN COLLECTOR TTL

In many applications open collector TTL-gates are used because it simplifies the design and reduces the cost. However propagation delay time gets increased and hence speed degrades. An open collector TTL NAND gate is shown in the Fig 3.8(a).

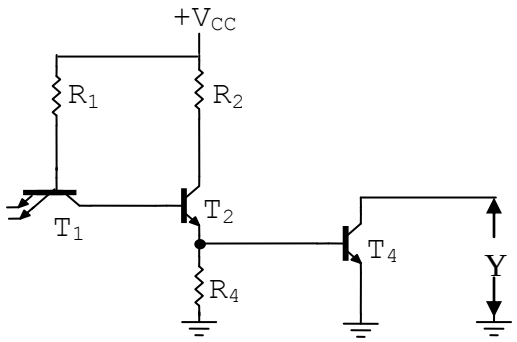


Fig.3.8 (a) : Open collector TTL

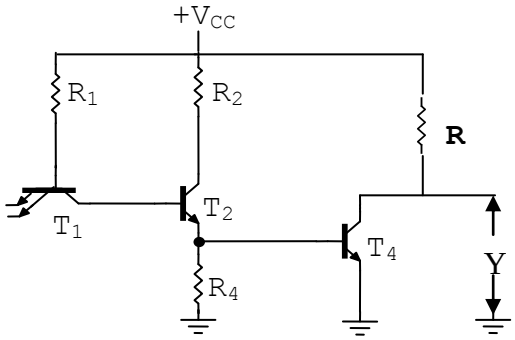


Fig.3.8 (b) : TTL NAND gate with pull up Resistor

In this circuit the upper transistor called *Active Pull Up Transistor* T_3 has been removed from the totem-pole pair of transistors in the output-stage. The output of such a circuit remains low, but switching from low to high state is not possible. For this purpose a high resistance (R) is connected between the collector of T_4 and V_{cc} as shown in Fig.3.8 (b).

When the T_4 goes to cut off the output is raised or pulled up to high voltage due to this resistance. Hence it is called as *Passive Pull-Up Resistor*. With this resistor the switching from low to high state becomes possible. However, the output resistance remains high, thereby increasing the propagation delay that ultimately reduces the speed of operation.

Use of Open Collector TTL

To produce 'OR'ing effect of many inputs an OR-gate with that many inputs is required. This increases the circuit's cost. But open collector circuit with common pull-up resistor produces the 'OR'ing effect as illustrated in figure.

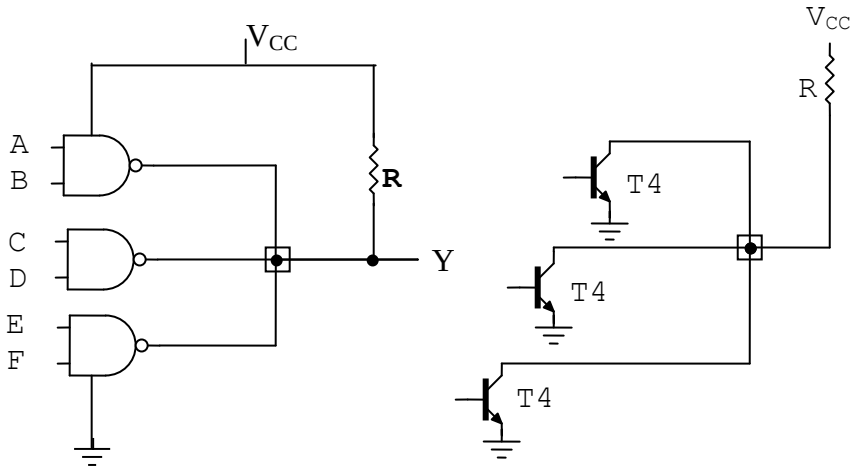


Fig.3.9: 'OR' ing effect of Open collector TTL

Since 'OR'ing has come through wiring of outputs together, it is known as *Wire-OR-Gate*.

Advantage and Disadvantages

The advantage of open collector TTL circuit is that it eliminates the need of separate OR-gate when 'OR'ing of signals are required.

However use of passive pull-up resistor increases the propagation delay. This considerably slows down the speed of operation. Also the capacitive load takes longer time to switch from low to high state

3.6 TRI-STATE LOGIC

In tri-state logic system a third state called as '*floating*' or '*high-impedance*' state is introduced in addition to high and low states. In the floating state the device remains electrically open, but not physically disconnected. This is used in computers or microprocessor based systems, where many I/O devices are connected to the common bus. C.P.U. Communicates with single I/O device keeping other in the floating-states.

3.6.1 TSL-Inverter

It is shown in the Fig.3.10. The TSL-Inverter has a controlling signal connected as Enable-signal (E). 'A' is an input signal and 'Y' is the output.

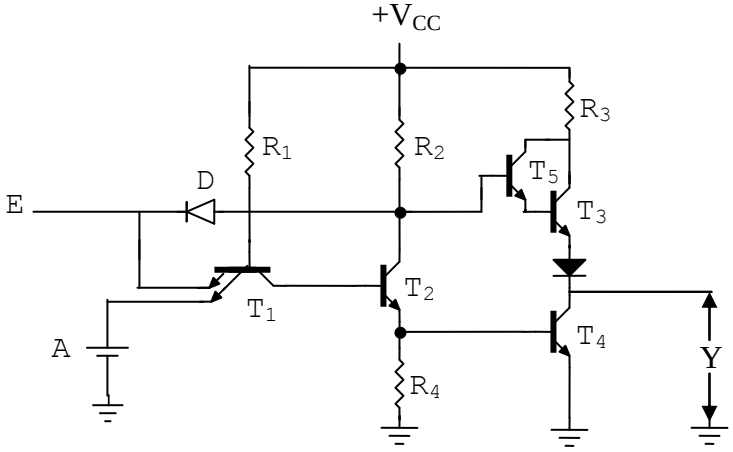


Fig 3.10: TSL Inverter

Working

Case 1: E = 0 (Low)

With enable input low, the diode D is forward biased. Hence the collector of T_2 is grounded. It remains cut-off irrespective of status of input signal (A). Due to this the transistors T_4, T_5 and T_3 remain cut-off. As T_3 and T_4 remain-Cut-off, the output Y therefore remains neither connected to Vcc nor connected to the ground. i.e. it remains in floating state or high impedance state.

Case 2: E=1 (High)

With enable signal high (E=1) the diode D is reverse- biased the short circuit at collector of T_3 gets removed. Therefore the circuit operates as a normal inverter. When input A is low, the transistor T_1 conducts, its collector voltage of T_2 turns the transistor T_5, and hence T_5 ON. While transistor T_3 remains cut-off. Hence output goes to high.

Where as when the input is 'A' is high, the transistor T_1 remains cut-off. The high emitter voltage of T_2 turns T_3 ON. The low collector voltage of T_2 turns T_5 and hence T_4 OFF. The output Y therefore goes low.

The action is summarized in the truth table as shown in Table 3.6.

Table 3.6: Truth Table of TSL Inverter

Enable E	Input A	Output Y
0	X	Z
1	0	1
1	1	0

X = don't care condition

Z = Floating or High Impedance Condition

Symbols-

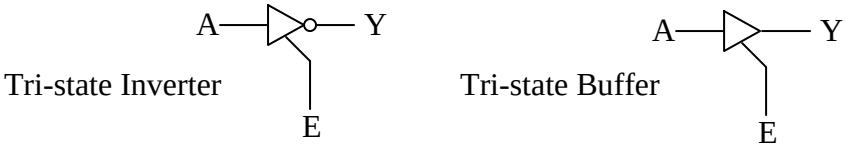


Fig.3.11: Symbols

Applications

- Totem pole outputs can be connected together as such a connection draws excessively large current and may damage the IC.
- Open Collector TTLs creates the loading problem and also degrades the speed. To overcome these difficulties Tristate Logic is used.

3.7 MOS [*METAL OXIDE SEMICONDUCTOR*] –TECHNOLOGY

The technology which uses MOSFETs is knows as MOS-technology. It is has following advantages-

1. Fabrication of MOS devices is easy and
2. It is possible to have high density of component-fabrication.
3. The MOSFETs draw negligibly small current when operated in complementary symmetry mode. Hence possess lower power consumption.

MOSFETs– Symbols and Working

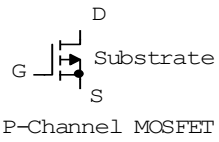


Fig 3.12(a): P-Channel MOSFET

P-Channel MOSFET is ON when gate voltage [V_G] = 0 Ve and it OFF when gate voltage [V_G] = + V.

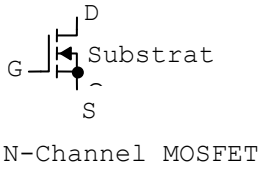


Fig 3.12(b): N-Channel MOSFET

N-Channel MOSFET is ON when gate voltage [V_G] = + Ve and it OFF when gate voltage [V_G] = 0 V.

3.7.1 CMOS-Inverter

Inverter constructed using P-MOSFET as a load in series with N-MOSFET or vice-versa to form complementary pair is known as CMOS-Inverter. This is shown in Fig 3.13.

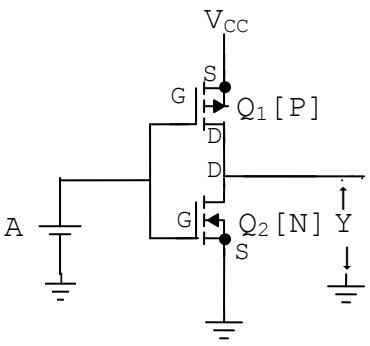


Fig 3.13: CMOS-Inverter

Case 1: A = 0 (Low)

With input a low, the p channel MOSFET Q_1 turns ON and N-channel MOSFET Q_2 OFF. Therefore voltage at D is raised almost to V_{DD}. The Y thus goes high.

Case 2: A = 1 (High)

With input A high the MOSFET Q_1 is OFF and Q_2 is ON. Conducting FET Q_2 grounds the voltage at D. The output Y thus goes low.

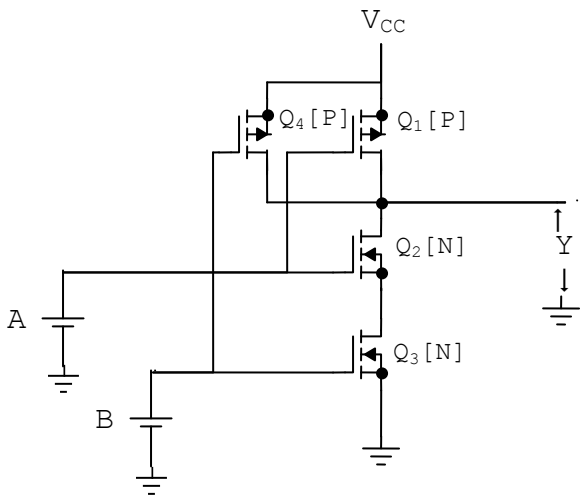
In this way the circuit operates as an inverter. As

one of the transistor remains OFF, the current drawn by the inverter either in low or high state is negligibly small. Hence the average power dissipation is minimum. It consumes power in nano-walls (nW).

But due increase in resistance, the propagation delay is high. Hence use of CMOS- gates is limited to low frequency applications.

3.7.2 CMOS NAND Gate

It is shown in the Fig.3.14. Its working can be explained under four cases.



Case 1: A = B = 0

With both inputs A and B low, P-channel MOSFETs Q_1 and Q_4 are turned ON. While N-channel MOSFETs Q_2 and Q_3 are cut-off. As Q_2 and Q_3 are cut-off, the voltage at output terminal is almost equal to V_{DD}, the output Y is raised to high state.

Case 2: A=0, B=1

With above input condition Q_1 & Q_3 are turned ON and Q_2 & Q_4 are cut-off. As Q_2 is cut-off and Q_1 is ON, the voltage at output terminal is almost equal to $V_{DD.}$ Thus the output Y is raised to high state.

Fig 3.14: CMOS NAND Gate

Case 3: A=1, B=0

With above input condition Q_2 & Q_4 are turned ON and Q_1 & Q_3 are cut-off. As Q_3 is cut-off and Q_4 is ON, the voltage at output terminal is almost equal to $V_{DD.}$ Thus the output Y is raised to high state.

Case 4: A=B=1

With both the inputs high both the P-channel MOSFETs Q_1 and Q_4 are turned ON and N-channel MOSFETs Q_2 and Q_3 cut-off. Therefore output Y is grounded through Q_2 and Q_3 and hence output goes low.

Action is summarized in truth table.

Table 3.7: Truth Table of CMOS NAND Gate

Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

3.7.3 CMOS NOR Gate

It is shown in the Fig 3.15.

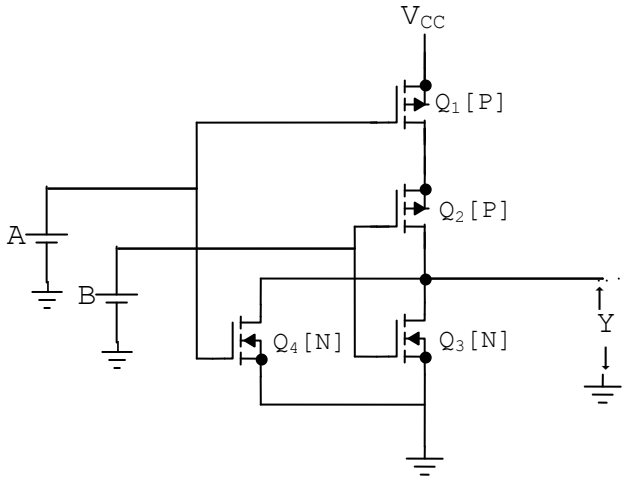


Fig.3.15: CMOS NOR Gate

Case 1: A = B= 0

With both the inputs low, P-channel MOSFETs Q_1 and Q_2 are turned ON. While N-channel MOSFETs Q_3 and Q_4 remain cut-off. As both Q_3 and Q_4 are off, the voltage at output terminal is almost equal to $V_{DD.}$ Thus output Y is raised to high state.

Case 2: A=0, B=1

With this input condition, MOSFETs Q_1 & Q_3 are turned ON, while MOSFETs Q_2 & Q_4 remain cut-off. The output Y is grounded through conducting transistor Q3 and hence output Y goes low.

Case 3: A =1, B=0

With this input condition, MOSFETs Q_2 & Q_4 are turned ON, while MOSFETs Q_1 & Q_3 remain cut-off. The output Y is grounded through conducting transistor Q_4 and hence output Y goes low.

Case 4: A=B=1

With both inputs high, N-Channel MOSFETs Q_3 and Q_4 are turned ON. While P-Channel MOSFETs Q_1 and Q_2 remain cut-off. The output Y is grounded through conducting Q_3 & Q_4 and hence output Y goes low.

Action is summarized in truth table as shown in Table 3.8.

Table 3.8: Truth Table of CMOS NOR

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

3.8. COMPARISON OF TTL AND CMOS LOGIC FAMILIES

Sr.No.	Parameter	TTL	CMOS
1.	Circuit	Transistor-transistor	Complementary MOS
2.	Basic Logic Function	NAND	Inverter
3.	Speed of Operation	More	less
4.	Propagation Delay per gate	4-12 ns	50 ns
5.	Power Dissipation per gate	10 mw	0.1 mw
6.	Nominal Supply voltage	5 V	3 to 15 Volt
7.	Wired Collector Capability	With passive pull up	With tristate output
8.	Fan out	10	50
9.	Noise Immunity	Good	Very good to excellent
10.	Compatibility with other families	With DTL	No, but compatible with TTL if supply is +5 V
11.	Available functions	Very High	High

Excercises

A) Multiple Choice Questions

1. The figure of Merit of a logic family is given by the product?
   a) Gain- bandwidth
   b) Propagation delay time and power dissipation
   c) Fan-out and propagation delay time
   d) Noise margin and power dissipation
2. As compared to TTL ,CMOS logic has
   a) high speed of operation
   b) higher power dissipation
   c) smaller physical size
   d) none of the above
3. For TTL IC noise margin is…….
   a) 0.4 V b) 0.8 v c) 0.5 v d) 1.0 v
4. The very large scale integration (VLSI) technology integrates _____ transistors
   a) 10000–1 million b) 100–1000 c) 1000–10000 d) 1 million–10 million

5. The CMOS logic family has……..
   a) low propagation time
   b) high power dissipation
   c) low fan in
   d) high fan out
6. In tristate logic when enable is equal to logic zero, then output is…….
   a) Low b) high c) high impedance d) low impedance
7. In open collector TTL NAND gate a……should used
   a) Pull-up resistor b) capacitor c) inductor d) none of these
8. In tristate logic third state is…….
   a) Low b) high c) high impedance d) low impedance
9. Noise margin is ……..
   a) Qualitative measurement of noise immunity
   b) Product of power dissipation and propagation delay time
   c) Both a and b
   d) none of these
10. For TTL IC power dissipation is …….
    a) 1 mw 2) 10 mw c) 15 mw d) 20mw

(B) Short Answer Questions

1. What is logic family? Give a different type of logic families.
2. Explain the characteristics of digital IC's
   a) Current and voltage parameters
   b) power dissipation
   c) Noise Margin
   d) Figure of Merit
   e) Propagation Delay time
   f) Fan In, Fan out
3. Explain the working of TTL NOT Gate (Inverter) with circuit diagram.
4. Explain the working of open collector TTL NAND Gate with circuit diagram.
5. Explain the working of tristate inverter with circuit diagram.
6. Explain the working of CMOS inverter with circuit diagram.
7. Give the comparison between TTL and CMOS logic families

(C) Long Answer Questions

1. Explain the working of CMOS NAND with circuit diagram.
2. Explain the working of CMOS NOR with circuit diagram.
3. Explain the working of TTL NAND Gate with circuit diagram.
4. Explain the working of TTL NOR Gate with circuit diagram.